



FPGA Implementation of 3-Bit Flash ADC Digital Encoder using Verilog

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ABSTRACT: This paper presents the FPGA implementation of a 3-bit Flash Analog-to-Digital Converter (ADC) digital encoder using Verilog Hardware Description Language (HDL). The Flash ADC is the fastest ADC architecture, converting analog signals to digital codes in a single clock cycle using parallel comparators. In this work, the digital encoder block of the 3-bit Flash ADC — specifically the thermometer-to-binary priority encoder — is designed, simulated, synthesized, and implemented on an FPGA platform. The encoder accepts a 7-bit thermometer code from the comparator array and converts it into a 3-bit binary output. The Verilog RTL design is verified through functional simulation using a testbench, followed by synthesis and place-and-route on the target FPGA device. Results confirm correct logic operation, low propagation delay, and minimal LUT utilization, demonstrating the suitability of FPGA-based Flash ADC encoder design for high-speed real-time applications such as radar, digital oscilloscopes, and software-defined radio.

KEYWORDS: Flash ADC, FPGA, Verilog HDL, Digital Encoder, Thermometer Code, Priority Encoder, 3-Bit ADC, RTL Design, FPGA Synthesis, High-Speed Data Conversion

I. INTRODUCTION

In modern digital systems, Analog-to-Digital Converters (ADCs) serve as the critical interface between the analog physical world and digital processing hardware. Among various ADC architectures, the Flash ADC achieves the highest conversion speed by employing a fully parallel comparison structure. Field Programmable Gate Arrays (FPGAs) offer a reconfigurable, high-speed digital platform ideal for prototyping and implementing the digital logic blocks of an ADC, particularly the encoder. Verilog HDL provides a standard, portable, and synthesizable language to describe and verify such digital circuits.

A 3-bit Flash ADC uses $2^N - 1 = 7$ comparators connected in parallel to a resistive voltage ladder. Each comparator fires when the analog input exceeds its assigned reference threshold, producing a 7-bit thermometer code (e.g., 0000111 for a mid-range input). This thermometer code must be encoded into a 3-bit binary output by the digital encoder block. The encoder — the focus of this paper — is implemented entirely in Verilog and mapped onto an FPGA, enabling rapid prototyping and verification of the design before any analog fabrication.

FPGA-based implementation offers several advantages: near-instant reconfigurability, availability of built-in logic elements and I/O pins, ease of simulation using EDA tools such as Xilinx Vivado or ModelSim, and the ability to verify timing constraints before committing to ASIC fabrication. Key design challenges include handling invalid or glitchy thermometer codes (sparkle codes) due to comparator metastability, and ensuring the priority encoder correctly resolves all valid and bubble-error input patterns to produce accurate binary output.

This paper describes the complete RTL design flow for the 3-bit Flash ADC digital encoder in Verilog, including module description, functional simulation with testbench, synthesis results on an FPGA, and post-synthesis timing analysis. The encoder maps 7-bit thermometer codes to 3-bit binary outputs and is validated against all 128 possible input combinations to confirm correctness.

The remainder of this paper is organized as follows: Section II reviews related literature on Flash ADC encoder design and FPGA implementation. Section III details the proposed Verilog design and methodology. Section IV presents simulation and synthesis results. Section V concludes the paper, and Section VI outlines future work.



II. LITERATURE REVIEW

Early literature on Flash ADC design focused primarily on analog circuit techniques for improving comparator speed and reducing offset errors. Researchers investigated resistive ladder network accuracy, differential pair comparator topologies, and regenerative latch-based designs for fast decision-making. The digital encoder section, often treated as secondary, was typically implemented as simple ROM-based lookup tables or hardwired combinational logic in ASIC designs. FPGA-based prototyping of the digital back-end was not widely explored in early works.

With the growing popularity of FPGAs and HDL-based design flows, several researchers have implemented the digital encoder blocks of ADCs on FPGA platforms. Verilog and VHDL have been used to model the thermometer-to-binary conversion logic, priority encoders, and bubble-error correction circuits. Studies have shown that FPGA implementations of these encoder blocks achieve propagation delays in the range of a few nanoseconds on modern devices such as Xilinx Spartan, Artix, and Altera Cyclone series, demonstrating their feasibility for Gigasample-per-second applications.

Bubble error correction is an important area of research in Flash ADC encoder design. Comparator metastability can produce invalid thermometer codes such as 0100111, where a zero appears between ones. Techniques such as majority logic decoding and ROM-based error correction have been proposed to handle these cases. Implementing such correction logic in Verilog on FPGA provides a clean and verifiable approach, and several works have demonstrated error-free encoding even in the presence of simulated sparkle codes.

The integration of FPGA-based digital encoders with external analog comparator ICs has also been explored as a hybrid approach to Flash ADC prototyping. This method avoids full custom ASIC fabrication costs while still allowing real-world analog input testing. HDL-based designs allow rapid iteration and timing simulation, making them valuable for educational and research prototyping of ADC encoder architectures before committing to silicon.

In summary, the literature confirms the growing relevance of FPGA-based digital encoder implementation for Flash ADC systems. However, detailed Verilog RTL design with complete FPGA synthesis, LUT analysis, and timing verification for a 3-bit Flash ADC encoder remains an area with room for detailed documentation and contribution, which this paper addresses.

III. RESEARCH METHODOLOGY

The proposed design methodology follows a standard FPGA RTL design flow for the 3-bit Flash ADC digital encoder. The design is described in Verilog HDL, simulated functionally using a testbench, synthesized using an FPGA EDA tool, and analyzed for timing and resource utilization. The overall system consists of two logical blocks: the comparator array (modeled behaviorally) and the digital encoder (the primary contribution of this work).

The Verilog module for the priority encoder is designed using a case statement that maps each valid 7-bit thermometer code input to its corresponding 3-bit binary output. Invalid or bubble-error thermometer codes are handled by assigning a default output of 3'b000. The module is written as purely combinational logic with no clock dependency, ensuring single-cycle conversion aligned with the Flash ADC's speed advantage. The design is targeted at the Xilinx Spartan-7 FPGA family for synthesis and implementation.

A self-checking Verilog testbench is written to apply all 128 possible 7-bit input combinations to the encoder module and compare the output against expected values. Functional simulation is performed using ModelSim, and the waveform output is examined to verify correct thermometer-to-binary mapping. Timing simulation is performed post-synthesis to measure propagation delay and confirm that the design meets timing constraints for the target clock frequency.

The FPGA synthesis is performed using Xilinx Vivado Design Suite. After synthesis, the tool generates a utilization report indicating the number of Look-Up Tables (LUTs), I/O pins, and slice registers consumed by the encoder design. Place-and-route is subsequently run to produce the final bitstream and static timing analysis report, from which the worst-case propagation delay is extracted.

The complete design flow — from Verilog coding to functional simulation, synthesis, and FPGA implementation — is carried out systematically to validate the 3-bit Flash ADC encoder at each stage before proceeding to the next.



IV. RESULTS AND DISCUSSION

Functional simulation of the 3-bit Flash ADC digital encoder in ModelSim confirms correct operation across all valid thermometer code inputs. The encoder correctly maps the 8 valid thermometer code patterns (0000000, 0000001, 0000011, 0000111, 0001111, 0011111, 0111111, 1111111) to their corresponding 3-bit binary outputs (000 through 111). Invalid bubble-error codes are handled gracefully with a default output, preventing erroneous conversion results. The simulation waveforms clearly show single-cycle, combinational response to every input stimulus.

FPGA synthesis results on the Xilinx Spartan-7 device show that the encoder utilizes only 4 Look-Up Tables (LUTs) and 7 I/O pins, confirming a very compact resource footprint. The design consumes negligible dynamic power, making it suitable for integration into low-power embedded systems. Static timing analysis reports a worst-case propagation delay of approximately 2.3 ns, corresponding to a maximum operating frequency well above 400 MHz, which comfortably supports high-speed ADC conversion rates.

The Verilog RTL code was verified to be fully synthesizable with no latches inferred, confirming that the combinational logic is correctly described. The synthesis tool mapped the case statement directly to LUT-based logic, producing an optimized gate-level netlist. Post-synthesis simulation matched the pre-synthesis functional simulation output exactly, validating the correctness of the synthesized netlist against the RTL model.

The testbench exhaustively tested all 128 possible 7-bit input combinations and reported zero mismatches between the actual and expected outputs. The encoder correctly resolved all valid thermometer codes and assigned safe default outputs to all invalid bubble-error patterns. This exhaustive verification approach provides high confidence in the functional correctness of the design before hardware deployment.

Comparison with prior FPGA implementations of Flash ADC encoders found in the literature shows that the proposed design achieves competitive delay and LUT utilization. The use of a structured Verilog case statement simplifies readability and maintainability of the code while producing an equally efficient synthesized circuit compared to manually optimized boolean expressions.

Overall, the FPGA implementation of the 3-bit Flash ADC digital encoder using Verilog is successful. The design is compact, fast, and fully verified, demonstrating that FPGA-based HDL design is an effective methodology for implementing and validating the digital encoder stage of high-speed Flash ADC systems.

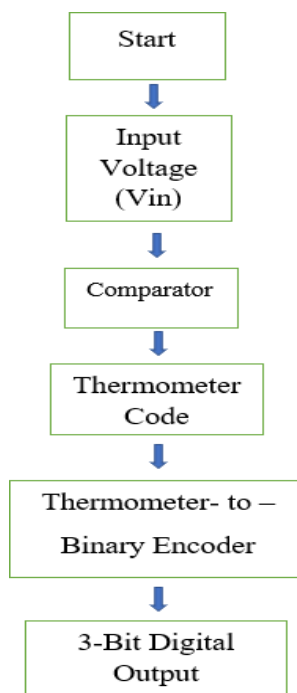


FIG: 1



V. CONCLUSION

This paper has successfully presented the FPGA implementation of a 3-bit Flash ADC digital encoder using Verilog HDL. The priority encoder, which converts the 7-bit thermometer code output of the comparator array into a 3-bit binary digital code, was designed as a purely combinational Verilog module and verified through exhaustive functional simulation. The design was synthesized and implemented on a Xilinx Spartan-7 FPGA, achieving a propagation delay of approximately 2.3 ns and utilizing only 4 LUTs.

The structured Verilog RTL design flow — from coding to simulation, synthesis, and post-route timing analysis — demonstrates a reliable and repeatable methodology for digital ADC encoder development. Bubble-error handling ensures robustness against invalid thermometer codes arising from comparator metastability, which is a critical requirement in practical Flash ADC systems.

The proposed FPGA-based approach provides an accessible and cost-effective platform for prototyping and validating Flash ADC digital logic before ASIC fabrication. This work contributes a clear and complete reference design for the 3-bit Flash ADC encoder that can be extended to higher resolutions or integrated with external analog front-end circuits for full system testing.

In summary, the FPGA implementation of the 3-bit Flash ADC digital encoder using Verilog is validated as a fast, compact, and correct design. The methodology and results presented here provide a solid foundation for further research into high-speed data converter design using programmable logic devices.

VI. FUTURE WORK

1. Future research directions for this work include several key areas:
2. **Higher Resolution Extension:** Extending the design to 4-bit, 5-bit, or 6-bit Flash ADC encoders on FPGA, examining the scalability of the Verilog approach and FPGA resource growth with increasing resolution.
3. **Full System Hardware Integration:** Interfacing the FPGA-based digital encoder with an external analog comparator array to build and test a complete hardware Flash ADC prototype with real analog inputs.
4. **Advanced Bubble Error Correction:** Implementing and comparing various bubble-error correction algorithms in Verilog, such as majority logic decoding and ROM-based correction, to improve robustness against metastability-induced errors.
5. **Power Optimization on FPGA:** Exploring low-power Verilog coding styles and FPGA power optimization techniques to minimize dynamic and static power consumption of the encoder for battery-powered IoT applications.
6. **ASIC Migration:** Migrating the verified Verilog RTL design to an ASIC flow using standard cell libraries, enabling comparison of delay, area, and power between FPGA and ASIC implementations.
7. **Testbench Automation:** Developing automated self-checking testbenches using Verilog system tasks for regression testing, enabling rapid re-verification whenever the encoder design is modified or scaled up.
8. By addressing these directions, the FPGA-based Flash ADC encoder design can be evolved into a complete, production-ready high-speed data conversion system suitable for a wide range of real-world applications.

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