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A Knowledge Enhanced Object Detection for Sustainable Agriculture

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ABSTRACT: Multilevel Inverters is a new breed of power converter that is suited for high voltage and high power applications. The various topologies of multilevel inverters are diode-clamped, and cascaded multilevel inverters. This project focuses on a H-bridge multilevel pulse width modulation converter topology based on a series connection of a high-voltage diode clamped inverter and a low voltage conventional inverter. A dc link voltage arrangement for the new hybrid and asymmetric solution is presented to have a maximum number of output voltage levels by preserving the adjacent switching vectors between voltage levels. Hence, a 15-level hybrid converter can be attained with a minimum number of power components. A new cascade inverter is verified by cascading an asymmetrical diode-clamped inverter, in which 19 levels can be synthesized in output voltage with the same number of components. a new multi-output boost converter is utilized at the dc link voltage of a seven-level H-bridge diode-clamped inverter. This paper involves the simulation of three phase 15-level and 19-level diode clamped multilevel inverter. Five level asymmetrical cascaded multilevel inverter employing Phase disposition (PD) PWM techniques are also investigated experimentally.

KEYWORDS- Asymmetrical diode clamped inverter, Hybrid cascade converter, Predictive current control

I. INTRODUCTION

Multilevel Inverters (MLI) have gained much attention in the field of the medium voltage and high power applications because of their many advantages, such as their low voltage stress on power switches, low harmonic and EMI output. Multilevel inverters are mainly utilized to synthesize a desired voltage wave shape from several levels of dc voltages. Multilevel inverter is an effective solution for increasing power and reducing harmonics of ac waveforms. Three topologies have been reported for multilevel inverters. They are Diode- clamped, flying capacitor and cascaded H-bridge. The main drawback of diode clamped inverter is the unbalanced dc link capacitor. Cascaded multilevel inverter has simple structure but it needs separate dc sources. A particular advantage of this topology is that the modulation, control and protection requirements of each bridge are modular. The complexity has generally restricted cascaded multilevel inverters to the higher power range where several switched output voltage levels are needed and diode clamped structure is unsuitable because of the difficulty of balancing the series dc capacitor voltages. A three phase 15-level and 19-level output is obtained from the series connection of seven level asymmetrical diode clamped H-bridge multilevel inverter with the multi-output boost converter and three level H-bridge inverter. A new multi-output boost converter is utilized at the dc link voltage of a seven-level H-bridge diode clamped multilevel inverter to balance the dc link capacitor voltages for the maximum output voltage resolution as well as to synthesize asymmetrical dc link combination.

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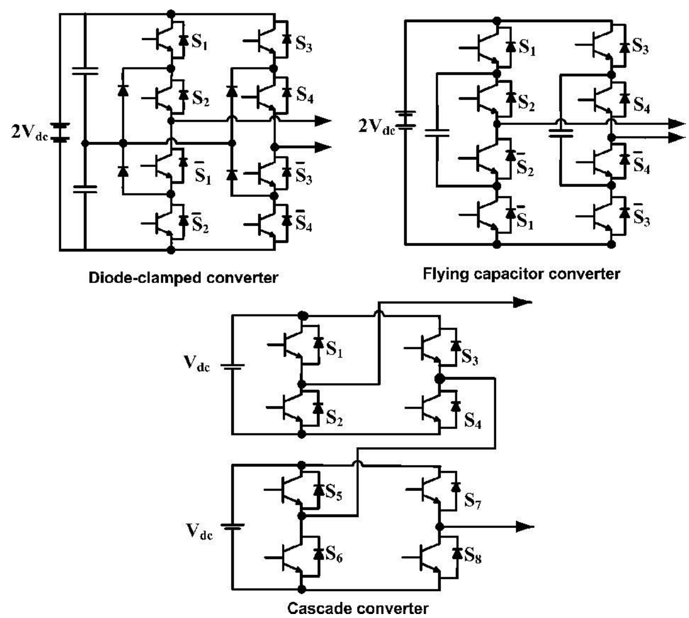

Fig. 1. Three multilevel topologies.

Typically, different types of multilevel converters are utilized with the same rating of the dc link voltages and power devices due to modularity and simplicity of the control strategy. Recently, asymmetrical multilevel inverters with unequal dc source voltages have been addressed in literature [9]–[30]. Therefore, based on different switching states, it is possible to achieve more voltage levels on output voltage by adding and subtracting dc link voltages compared with conventional multilevel inverters with the same number of components [9]. By doing so, output voltage with superior quality can be obtained with less circuit and control complexity, and also, increasing the harmonic characteristic of the output voltage can decrease.

The hybrid converters have been the main focus of the literature with regard to asymmetrical configuration of multilevel inverters as they have shown their abilities and strengths in medium- and high-power applications Diverse topologies have been studied based on a variety of H-bridge cascaded cells and dc voltage ratio to enhance the out-put voltage resolution compared with the same dc voltage ratio of the cells . However, due to the different voltage rates of switching devices in hybrid configuration, it loses its modularity compared with symmetrical cascade inverters. Various pulse width modulation (PWM) strategies for symmetrical cascade inverters with high and fundamental switching frequency have been presented . To reduce switching losses and improve the converter efficiency, hybrid modulations for cascade converters with unequal dc sources are proposed, which allows use of the slow switching device in the higher voltage cells and fast switching devices in lower voltage cells.

Since more voltage levels correspond to the increasing number of components, recent research in this area has focused on a series of connected multilevel converters in a cascaded H-bridge structure [28]–[30]. The structure of the cascaded multilevel inverter is demonstrated in Fig. 2, where the configuration consists of m-level multilevel H-bridge cells (either diode-clamped or flying capacitor inverter), each with an isolated dc source.

The number of cells depends on the desired output volt-age level, which is synthesized by adding up all the H-bridge cells output

$v_{out}(t) = v_{out1}(t) + v_{out2}(t) + v_{out3}(t)$

(t). In a system that utilizes equal sets of dc sources ($V_{dc1} = V_{dc2} = V_{dc3} = \cdots = V_{dcN}$), the number of output voltage levels is $N\times(m-1) + 1$, where N is the number of cascaded cells and m is the number of output voltage levels in each multilevel H-bridge cells. The main advantage of this arrangement is the simplicity to cascade several H-bridge cells for improvement of the output voltage resolution with reduced number of components. However, capacitor voltage imbalance and complexity of the system can cause a critical problem that should be taken into account in this configuration using either diode-clamped or flying capacitor topology [31], [35]. To address this limitation, isolated dc sources or, alternatively, auxiliary converters can be used for capacitor voltage balancing. Utilization of unequal dc sources on each series diode-clamped or flying capacitor cells can increase the number of output voltage for a given power circuit in Fig. 2, with the equivalent number of components. A different dc voltage ratio for H-bridge cells is proposed to achieve the maximum number of output voltage levels. However, along with possible maximization of obtainable output voltage levels based on the voltage ratio of dc sources, the existence of adjacent switching vectors to move from one possible voltage level to another with only one switch change should be considered. Simultaneous switching of different switches is not an immense problem when there are just a few of them happening over one cycle; however, when switching between the nonadjacent switching vectors occurs frequently in modulation between adjacent levels, it becomes a critical issue to increase the switching losses.

In this paper, a general idea of cascading multilevel H-bridge cells is used to propose different configurations using a seven-level symmetrical and asymmetrical diode-clamped H-bridge converter supplied with a multi-output boost (MOB) converter, cascaded with classical three-level inverters. The MOB converter can solve the capacitor voltage imbalance problem as well as boost the low output voltage of renewable energy systems such as solar cells to the desired value of the diode-clamped dc link voltage. Using a triple-output dc–dc converter offers asymmetrical dc link capacitor voltage arrangement for the seven-level H-bridge diode-clamped converter, in which nine voltage levels can be obtained with the same number of components. Using an asymmetrical diode-clamped converter in the proposed cascaded H-bridge cells achieves four more voltage levels in the output compared with the symmetrical configuration. Performance of the proposed asymmetrical H-bridge diode-clamped inverter has been verified by simulation and hardware results. Finally, two different PWM methods based on predictive current control have been presented to validate the proposed approach.

II. SYMMETRICAL AND ASYMMETRICAL DIODE-CLAMPED CONVERTERS (SDCC AND ADCC) USING THE MOB CONVERTER

A new dc–dc boost converter with multiple outputs, which can be used as a front-end converter to boost the inverter's dc link voltage for grid connection systems based on a diode-clamped converter, is analyzed in [35]. Using this MOB converter, the dc voltage across each capacitor can be adjusted to a desired voltage level, thereby solving the main problem associated with balancing the capacitors' voltages in such converters. In [11], a new modulation technique has been presented for a diode-clamped inverter when voltages across capacitors are unequal. Fig. 3 shows a configuration for an H-bridge seven-level diode-clamped inverter joint with the front-end MOB converter. An unequal dc link arrangement is applied instead of identical dc link capacitor voltages. The bottom capacitor's voltage is kept at twice the level of other capacitors during operation, so that the configuration has asymmetrical behavior with respect to the neutral point ($V_{c1} = 2V_{c2} = 2V_{c3}$

According to the structure of the seven-level diode-clamped converter, there are four possible switching states in each leg of the inverter that can be derived from four switch combinations to obtain different dc link voltage levels. The "ON" and "OFF" switching states of each switch are defined as "1" and "0," respectively. Four switching states in one leg of the diode-clamped H-bridge inverter are distinguished by four switching function states that are summarized in Table I. For example, (011) means that $S_1 = 0$ (OFF), $S_2 = 1$ (ON), and $S_3 = 1$ (ON), which is defined as switching function state "2."

All possible switching states associated with different output voltage levels in SDCC and ADCC are shown in Table II. Exploring the output voltage levels.

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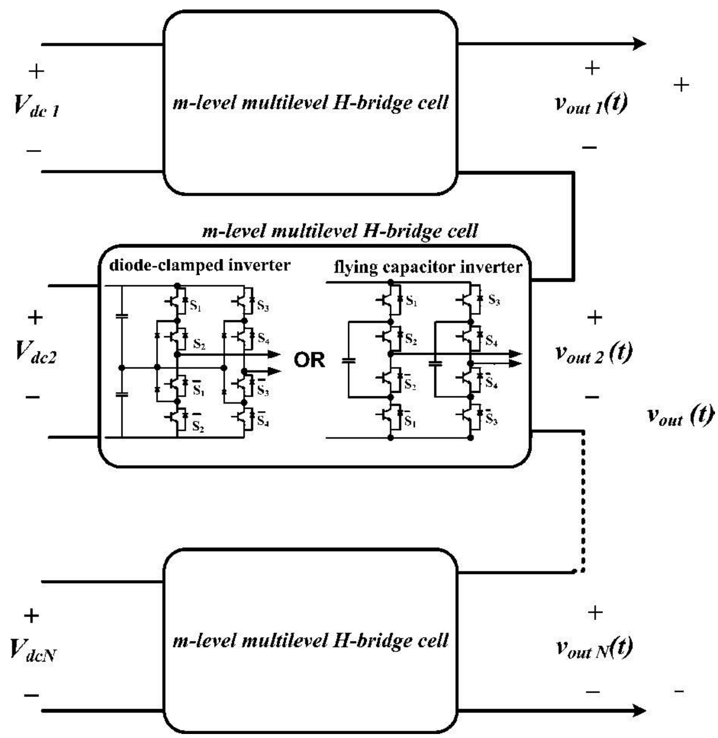

Fig. 2. Topology of the cascaded multilevel H-bridge converter.

TABLE I

Output Voltage Levels Associated With Different Switching Function States for SDCC and ADCC Configurations

Switching function states	S_1	S_2	S_3	S_7	S_8	S_9	*SDCC* (v_{out})	*ADCC* (v_{out})
00	0	0	0	0	0	0	0	0
01	0	0	0	0	0	1	$-V_{dc}/3$	$-V_{dc}/2$
02	0	0	0	0	1	1	$-2V_{dc}/3$	$-3V_{dc}/4$
03	0	0	0	1	1	1	$-V_{dc}$	$-V_{dc}$
10	0	0	1	0	0	0	$V_{dc}/3$	$V_{dc}/2$
11	0	0	1	0	0	1	0	0
12	0	0	1	0	1	1	$-V_{dc}/3$	$-V_{dc}/4$
13	0	0	1	1	1	1	$-2V_{dc}/3$	$-V_{dc}/2$
20	0	1	1	0	0	0	$2V_{dc}/3$	$3V_{dc}/4$
21	0	1	1	0	0	1	$V_{dc}/3$	$V_{dc}/4$
22	0	1	1	0	1	1	0	0
23	0	1	1	1	1	1	$-V_{dc}/3$	$-V_{dc}/4$
30	1	1	1	0	0	0	V_{dc}	V_{dc}
31	1	1	1	0	0	1	$2V_{dc}/3$	$V_{dc}/2$
32	1	1	1	0	1	1	$V_{dc}/3$	$V_{dc}/4$
33	1	1	1	1	1	1	0	0

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TABLE III
Maximum Voltage Rate across Switching Components In One Leg Of A Seven-Level H-Bridge Diode-Clamped Inverter With Symmetrical And Asymmetrical Dc Link Arrangements

Switching components	Max. voltage rating of SDCC	Max. voltage rating of ADCC
S_1	$V_{dc}/3$	$V_{dc}/3$
S_2	$V_{dc}/3$	$V_{dc}/3$
S_3	$V_{dc}/3$	$V_{dc}/2$
S_4	$V_{dc}/3$	$V_{dc}/3$
S_5	$V_{dc}/3$	$V_{dc}/3$
S_6	$V_{dc}/3$	$V_{dc}/2$
D_{c1}	$V_{dc}/3$	$V_{dc}/4$
D_{c2}	$2V_{dc}/3$	$3V_{dc}/4$
D_{c3}	$2V_{dc}/3$	$V_{dc}/2$
D_{c4}	$V_{dc}/3$	$V_{dc}/2$

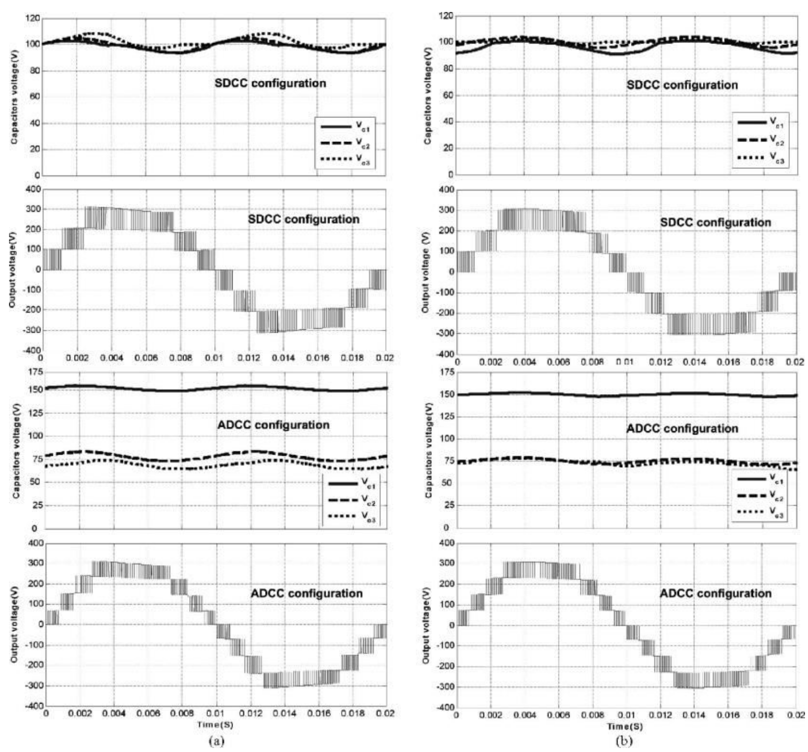

Fig. 5. DC link capacitor voltages and output voltage for SDCC configuration and ADCC configuration with (a) resistive load (ma = 1, PF = 1) and (b) inductive load (ma = 1, PF = 0.5).

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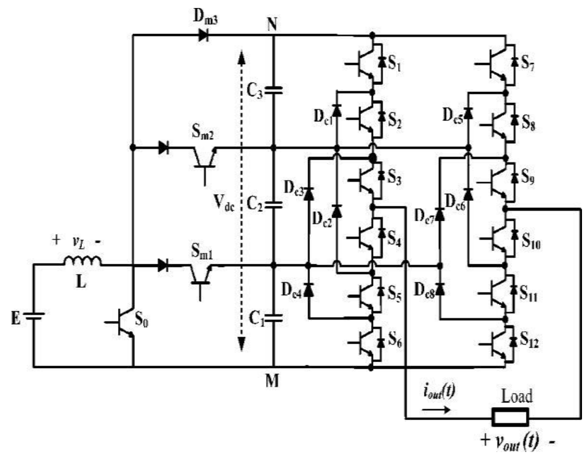

Fig. 3. H-bridge proposed diode-clamped inverter with three dc link capacitors joint with a triple-output boost converter.

switching transitions in the ADCC configuration, which are depicted by dashed lines in Fig. 4:
1) (20) and (31)
2) (02) and (13).

This transition requires two switch changes in the ADCC. To remove nonadjacent voltage vector in positive voltage levels, when the controller increases the voltage level from V_{dc} /2 to 3V_{dc} /4, transition occurs from switching function states (31) to (20). Then, the controller uses switching function state (10) for modulation between V_{dc} /2 and 3V_{dc} /4. Also, after the occurrence of the transition from 3V_{dc} /4 (20) to V_{dc} /2 (31), the controller uses state (21) for the modulation between V_{dc} /2 and V_{dc} /4. The same situation happens when the output voltage is negative. Therefore, these nonadjacent switching transitions occur only four times during one cycle. It is apparent that by assuming that switching losses are proportional to the number of switching per cycle, the switching loss associated with the extra switching is negligible at high switching frequency. As a result, improved voltage waveforms can be obtained using ADCC topology compared with SDCC topology with the same number of components and almost the same number of switching's. Although the output voltage of the asymmetrical dc link arrangement benefits from two more voltage levels with the same number of components compared with the symmetrical dc link arrangement, extra voltage rates should be taken into account for two switches in each leg of the inverter. Maximum voltage across switching components during different switching states is derived in Table III to have a comparison between the volt-age rating in the symmetrical and asymmetrical dc link arrangements. In the asymmetrical configuration, the maximum voltage rating of switches (S_3 and S_6) in each leg is V_{dc} /6 more than the switches in the symmetrical configuration for the same dc link voltage. By investigating the voltage ratings, maximum voltage rating of diodes (D_{c1} and D_{c3}) decreased by V_{dc} /12 and V_{dc} /6; however, the maximum voltage tolerated by another two diodes (D_{c2} and D_{c4}) increased by V_{dc} /12 and V_{dc} /6, which shows that the maximum voltage across diodes has not changed in both configurations. The output voltage of the symmetrical and asymmetrical single-phase diode-clamped inverters for the same circuit parameters is shown in Fig. 5. Herein, at the dc–dc side, input volt-age (E) is assumed to be 100 V; switching frequency of the dc–dc converter (f_{sw}) is 10 kHz, L = 2 mH, and $C_1 = C_2 = C_3$ = 1 mF, while at the inverter side, fundamental and switching frequencies are f = 50 Hz, f_{sw} = 4 kHz, and the dc link of the seven-level diode-clamped inverter (V_{NM}) is boosted to 300 V using a triple-output boost converter. Midpoint voltage regulation for symmetrical and asymmetrical configurations for high modulation index (m_a = 1) and unity power factor (PF) has been shown in Fig. 5(a). It is clear that the MOB converter is able to boost the low input

voltage for dc link capacitors as well as balance the capacitors voltage to the desired level for m_a = 1 and pure resistive load, which is impossible in more than five-level single-phase diode-clamped topology without an active front-end converter. In order to generate the output volt-age, based on the duty cycle of switches, the controller chooses the next suitable switching function state using the adjacent vectors in Fig. 4. To show the performance of the proposed

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structure for inductive load, Fig. 5(b) illustrates the dc link capacitor voltage control and output voltage for $m_a = 1$ and PF = 0.5. In order to synthesize an equal dc link capacitor voltage arrangement in the conventional configuration, while the total voltage of an inverter dc link is boosted at 300 V, midpoint voltages (V_{c1} and $V_{c1} + V_{c2}$) are controlled at 100 and 200 V. However, to have an asymmetrical dc link configuration, midpoint voltages are controlled at 150 and 225 V, respectively.

A laboratory prototype of a symmetrical and an asymmetrical seven-level H-bridge inverter has been implemented to practically verify the proposed configuration. The laboratory proto-type has been tested for the following specifications: V_{dc} = 90 V, $I_{ut\text{-}peak}$ = 5 A, f = 160 Hz, and f_{sw} = 6 kHz under pure inductive load L = 16 mH. A predictive current control has been developed in a V850E/IG3 microcontroller to force the load cur-rent to follow the for the H-bridge seven-level diode-clamped inverter with symmetrical and asymmetrical dc link arrangements. Switching states to generate the desired voltage level based on the amount of current reference is chosen by the microcontroller according to adjacent switching vectors. Output voltage and current of the symmetrical and the asymmetrical seven-level diode-clamped inverter is demonstrated in Fig. 6. Regarding simulation and hardware results, two more voltage levels can be synthesized in output voltage of the ADCC configuration compared with the SDCC configuration with the same number of components and structure. Therefore, the seven-level H-bridge inverter performs similarly to a nine-level inverter. To examine the performance of the asymmetrical configuration, harmonic spectrums associated with the output voltage of both the SDCC and ADCC configurations are exposed in Fig. 6. Comparing harmonic spectrums, better harmonic performance is obtainable using the asymmetrical dc link arrangement for the diode-clamped converter. This achievement allows, on one hand, an improvement in output voltage harmonic characteristics with the same number of components compared with the symmetry-cal seven-level H-bridge configuration, and on the other hand, a decrease in cost and complexity of the inverter hardware lay-out structure with the same output waveforms quality compared with the symmetrical nine-level H-bridge inverter.

III. PROPOSED MULTILEVEL HYBRID CASCADE CONVERTERS

One of the aspects of this paper is to select dc input voltages for a topology based on a series connection of a symmetrical and an asymmetrical diode-clamped H-bridge cell with three-level H-bridge inverters to achieve a maximum number of output levels by preserving the minimum switching losses. Simultaneous switching of different switches is not a real problem when there are just few of them happening over one cycle; however, repeatedly switching between the nonadjacent switching vectors is not acceptable, due to an increase in switching losses and com-mutation noise. The state of art in this topology can improve the resolution of the output voltage with minimum power components, while keeping the adjacent switching vectors between all modulation voltage levels. Fig. 7 presents the schematic of this configuration for a two-cell hybrid cascade converter. The MOB converter is utilized to supply dc input voltage of the diode-clamped multilevel H-bridge cell to regulate capacitors voltages and provide the desired voltage rate for the dc link capacitors.

V. CONCLUSION

This paper has presented the diode-clamped multilevel H bridge cell cascaded with three-level conventional inverters to increase efficiency of converters with high output voltage resolution. A novel dc link voltage rating is proposed for the multilevel diode-clamped and three-level H-bridge inverters to improve the output voltage and current quality by preserving the adjacent switching vectors between all voltage levels. The MOB converter has been applied as a dc link supplier of a diode clamped inverter to boost and regulate the capacitors' voltage to the desired dc link rates. Using the MOB converter, a new cascade inverter is verified by cascading asymmetrical seven-level H-bridge diode clamped inverter. Inverter with nineteen output voltage levels performance was achieved, which has more voltage levels as well as lower voltage, and current THD rather than using a symmetrical diode-clamped inverter with the same configuration and equivalent number of power components. Predictive current control was conducted to show the performance of the proposed method. In this case, two different methods for the switching states selection are proposed to minimize either losses or THD of voltage in hybrid converters. Novel H-bridge cascaded cells will decrease the complexity of control and cost of the system as well as diminish or remove the output filters when the configuration will be extended for more H-bridge cells.

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