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Leakage Power Reduction through Hybrid Multi-Threshold CMOS Stack Technique

Dr.C.Nagarajan[1], Thilothammal.A[2], V.Anandhapriya[3], S.Logapreethi[4], M.Mounika[5]

Muthayammal Engineering College, Rasipuram, Tamil Nadu, India[1]

Department of Electronics and Communication Engineering, Muthayammal College of Engineering, Rasipuram, Tamil Nadu, India[2-5]

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ABSTRACT: In this paper, two hybrid digital circuit design techniques, namely, hybrid multi-threshold CMOS complete stack technique, hybrid multi-threshold CMOS partial stack technique, have been proposed to reduce the subthreshold leakage power dissipation in standby modes. Techniques available in literature are compared with our proposed hybrid circuit design techniques. Performance parameters such as subthreshold leakage power dissipation in active and standby modes, dynamic power dissipation and propagation delay, are compared using existing and proposed hybrid techniques for a some testing circuits. Reduction of subthreshold leakage power dissipation in standby mode is given more importance, in comparison with the other circuit design performance parameters. The proposed hybrid stack technique proved to perform better in terms of subthreshold leakage power dissipation in standby mode in comparison with other techniques. Simulation results using cadence virtuoso tool in 180 nm CMOS technology is provided in this paper.

KEYWORDS: Subthreshold Leakage Power; Standby Mode; Active Mode; Propagation Delay

I. INTRODUCTION

Design of low power circuit is necessary for portable electronic devices that are powered by batteries as in- creased power dissipation reduces the battery lifetime. Low power dissipation by MOS transistors and its small size for greater integration capacity are the major factors behind shifting in technology from BJTs to MOSFETs. High power dissipation is one of the major challenges of integrated circuit design in deep submicron and nanoscale technologies [1-5]. The demand for higher functions with higher performance and lower power dissipation initiates the scaling of MOS transistors in every technology generations. The contribution of dynamic power in the overall power dissipation decreases with the scaling of MOS transistors. Leakage power is expected to increase 32 times per device by the year 2020 [6]. Reduction of the supply voltage, *VDD* is considered as the most effective method to reduce the dynamic power, which is directly proportional to the square of the supply voltage, *VDD*. In order to maintain the same performance, threshold voltage of the transistor is also reduced with the scaling of the supply voltage. However, subthreshold leakage current increases exponentially with the reducetion of the threshold voltage of the MOS transistor, making it critical for low voltage digital integrated circuit design. Scaling of transistors in every technology generations also lead to increase in the subthreshold leakage current. With rapid scaling in technology, the increase in leakage current has made leakage power a significant part in the overall power dissipation in both active and standby modes. The major components of leakage power dissipation are subthreshold leakage, gate leakage, gate induced drain leakage, and forward biased diode leakage [7]. Subthreshold leakage dominates the other leakage components in deep submicron and nanoscale technologies.

Threshold voltage of transistors used in design of dig-ital circuits should be adjusted for maximum saving in the leakage power dissipation.Circuit techniques play a very important role to control the subthreshold leakage power dissipation in both active and standby modes. Already some techniques, such as Multi-threshold CMOS(MTCMOS) technique [8,9], Stack technique [11-13] and Sleepy stack technique [14] are available in literature to control the subthreshold leakage power dissipation in deep submicron and nanoscale technologies. Each technique has its own advantages and disadvantages. Depending upon the requirement and application, chip designers can choose the appropriate circuit design technique.

In this paper, two new digital circuit design techniques namely, hybrid multi-threshold CMOS complete stack technique, hybrid multi-threshold CMOS partial stack technique,are presented. These techniques are applied to a testing circuits to evaluate their performance. It is found that the proposed techniques give improved performance in terms of reduced subthreshold leakage power dissipation in standby mode as compared with the other techniques available in the literature [8-14].

II. SUBTHRESHOLD LEAKAGE POWER DISSIPATION

Subthreshold or weak inversion conduction current is the current flow between source and drain region in a MOS transistor, even when gate voltage, *VGS* is below the threshold voltage, *VTH* of the MOS transistor. It is due to the minority carrier drift through the channel from the drain to the source region in weak inversion region. **Figure 1** shows the flow of subthreshold leakage current in an nMOS transistor, when *VGS* is less than *VTH* of the transistor. **Figure 2** [15] shows the variation of minority carrier concentration along the length of the channel for an n-channel MOSFET biased in the weak inversion region. This figure shows that the concentration of minority carriers in weak inversion region is small, but not zero. Subthreshold leakage power dominates the other leakage power components because of the necessity to use low threshold voltage transistors to maintain the desired performance of the device. This leakage power should be minimized through new and improved circuit design techniques. This leakage power dissipation is undesirable in digital circuit design.

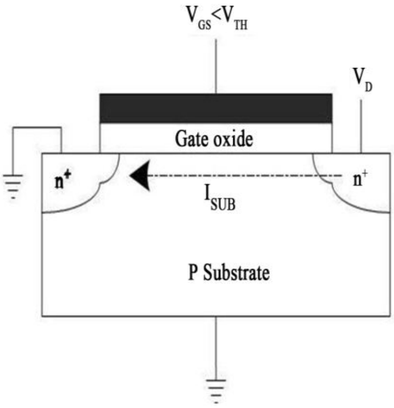


Figure 1. Subthreshold leakage current in an nMOS transistor.

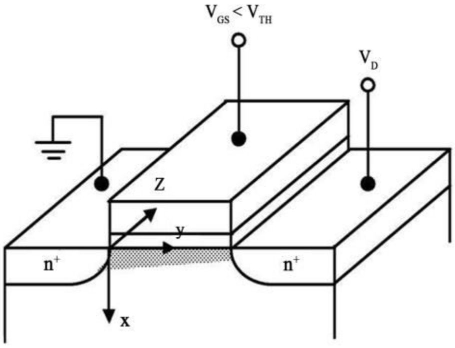


Figure 2. Variation of minority carrier concentration in an nMOS transistor in weak inversion.

III. CIRCUIT DESIGN METHODOLOGY ADOPTED FOR REDUCING SUBTHRESHOLD LEAKAGE POWER IN STANDBY MODE

Subthreshold leakage power reduction in standby mode is significant in burst mode type circuits, where computation occurs only during short burst intervals, and the system is in standby mode for the majority of the time [18]. The wastage of useful battery power during long standby period is highly undesirable. New circuit techniques must be devised to control the subthreshold leakage power dissipation in standby mode for burst mode applications. Portable battery operated devices that remain in standby mode for most of the times are greatly affected by standby subthreshold leakage power loss. Existing circuit design techniques must therefore be modified in such a way that it curbs the draining of battery current when it is not operational. **Table 1** [19] shows the dependence of subthreshold leakage current on MOS device parameters. Increasing the threshold voltage of the MOS transistor is an effective way to reduce subthreshold leakage power dissipation. Stack effect or Self-Reverse bias effect is the phenomenon where subthreshold leakage current decreases due to two or more series connected turned off transistors. Stacking of transistor is done by replacing transistor of width W with two series connected transistors of width W/2. **Figure 3** shows the natural stacking of nMOS transistors in a two input NAND gate. When both nMOS transistors *Q*1 and *Q*2 are turned off, then the intermediate node voltage, *VQ* raises to a positive value due to the presence of a small drain current.

Table 1. Dependence of subthreshold leakage current on MOS transistor parameters

Transistor parameter	**Dependence of subthreshold leakage**
Transistor width (W)	Directly proportional
Transistor length (L)	Inversely proportional
Temperature (T)	Exponential increase
Transistor threshold voltage (*VTH*)	Increases by an order of magnitude with 100 mV decrease
Input voltage (*VGS*)	Exponential increase

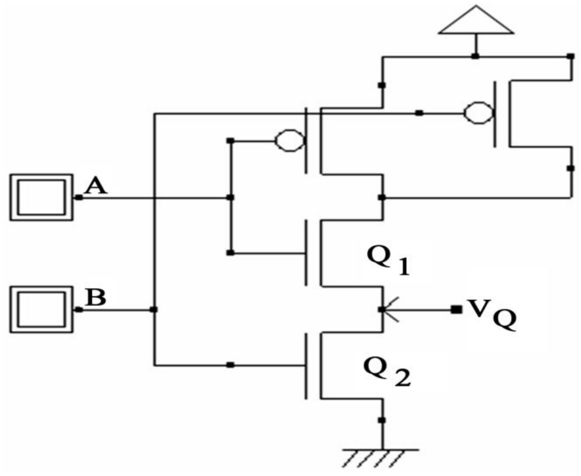


Figure 3. Natural stacking of nMOS transistors in a two input NAND gate.

At the intermediate node between two turned off stacked transistors has following effects [19,20]:
1) *VGS* of *Q*1 becomes negative;
2) *VBS* of *Q*1 becomes negative, causing an increase in *VTH* of *Q*1 due to an increase in the body effect of *Q*1;
3) *VDS* of *Q*1 decreases, resulting in less drain induced barrier lowering.

IV. PROPOSED HYBRID CIRCUIT TECHNIQUES

In this section, we propose four new digital circuit techniques namely, hybrid MTCMOS complete stack technique, hybrid MTCMOS partial stack technique,for the reduction of sub- threshold leakage power dissipation in standby modes. First two techniques are grouped as hybrid MTCMOS stack Proposed techniques are discussed as follows.

4.1. Hybrid Multi-Threshold CMOS Stack Technique

This technique combines the advantages of both MTCMOS and Stack techniques. This proposed hybrid technique is further classified, as given above, into two types depending on the stacking of transistors.

4.1.1. Hybrid Multi-Threshold CMOS Complete Stack Technique

The proposed logic circuit for hybrid MTCMOS complete stack technique is shown in **Figure 4**. In this tech nique, a high threshold voltage pMOS transistor (sleep pMOS transistor) is inserted between *VDD* and the pull up network and a high threshold voltage nMOS transistor (sleep nMOS transistor) is inserted between the pull down network and GND. Then stacking of all transistors (high *VTH* sleep pMOS, high *VTH* sleep nMOS and low *VTH* transistors of the logic circuit) are done by replacing each transistor of width *W* with two series connected transistors of width W/2. During standby mode, the sleep signal is active high, making the stacked sleep transistors in cutoff state. So, the logic circuit is disconnected from *VDD* and GND. This reduces the subthreshold leakage power dissipation significantly by utilizing stacking effect in both high *VTH* sleep nMOS and sleep pMOS transistors during their cutoff states. The high *VTH* nMOS and pMOS stacked sleep transistors are turned on during normal or active circuit operation, when the sleep signal is active low.

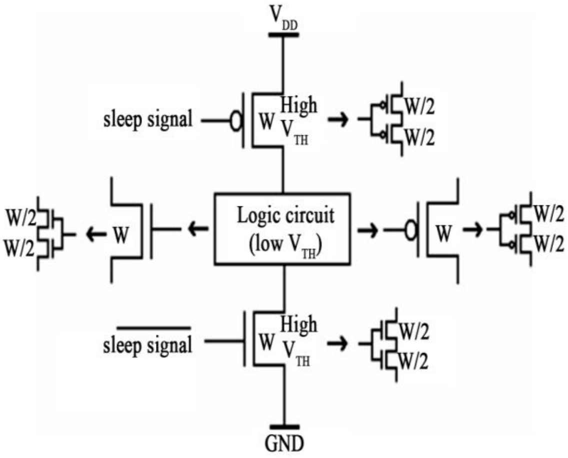
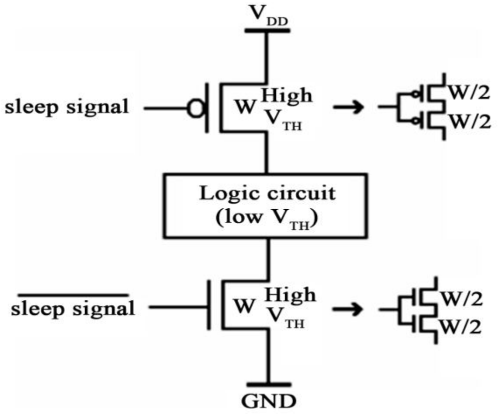


Figure 4. Logic circuit using hybrid MTCMOS complete stack technique.

4.1.2. Hybrid MTCMOS Partial Stack Technique

The proposed logic circuit for hybrid MTCMOS partial stack technique is shown in **Figure 5**. In this technique, a high *VTH* pMOS transistor (sleep pMOS transistor) is inserted between VDD and the pull up network and a high *VTH* nMOS transistor (sleep nMOS transistor) is inserted between the pull down network and GND. Then stacking of only high *VTH* sleep pMOS and high *VTH* sleep nMOS transistors are done



In this technique, stacking of low *VTH* nMOS and pMOS transistors of the logic circuit is not performed. Here, only partial stacking of high *VTH* sleep pMOS and sleep nMOS transistors are done to reduce the overall circuit propagation delay in active mode. During standby mode (when sleep signal is active high), the stacked high *VTH* sleep pMOS and sleep nMOS transistors are turned off, thereby, reducing significant sub- threshold leakage power dissipation. In active mode, the stacked sleep transistors are turned on. The circuit propagation delay using this technique in active mode is slightly reduced as compared to the previous technique because of partial stacking of transistors (stacking of only sleep pMOS and sleep nMOS transistors).

V. RESULT AND DISCUSSION

To compare the performance, the proposed techniques are applied to a some testing circuits. The performance parameters such as subthreshold leakage power dissipation in active and standby modes, dynamic power dissipation and propagation delay of a testing circuits were analysed in 180 nm technology using existing [10-16] and proposed hybrid techniques. The threshold voltage of high *VTH* transistor was taken as two times of *VTH* of normal transistor of the logic circuit. The threshold voltage of normal nMOS and pMOS transistors (low *VTH*) were taken as 0.20 V and −0.20 V respectively.

Subthreshold leakage power dissipation was measured by combining all possible input vectors. The voltage magnitude of input vector should always be less than the threshold voltage of the normal transistor of the logic circuit. Sleep nMOS and sleep pMOS transistors were turned off during measurement of subthreshold leakage power dissipation in standby mode while for its measurement in active mode, all sleep nMOS and sleep pMOS transistors were turned on.
Dynamic power dissipation was measured by applying input pulse signals of same frequency with a fixed delay between them. Two input pulse signals of *VDD* of 0.7 V and frequency of 250 MHz were applied to a two input AND gate. All sleep nMOS and sleep pMOS transistors were turned on during measurement of dynamic power dissipation. The dynamic power dissipation was measured for a testing circuit 50 ns time interval. Propagation delay of the logic circuit was measured from the trigger input edge reaching 50% of *VDD* to the circuit output edge reaching 50% of *VDD*.

Hybrid stack technique are tested by some benchmark circuits in the cadence virtuoso tool at 180nm technology and calculated the leakage power and delay shown in **Table2.**

Technique	**Leakage current (mA)**		**Dynamic power(mW)**	**Delay(ns)**
	active	**standby**		
MTCMOS	3.79	2.546	3.651	2.6
Hybrid MTCMOS complete stack	2.73	2.321	1.68	1.9
Hybrid MTCMOS partial stack	2.63	1.963	1.39	1.7

From these result the proposed hybrid super cutoff stack technique proved to perform better in terms of subthreshold leakage power dissipation in standby mode in comparison with other techniques. Although dynamic power dissipation is slightly higher, the proposed technique is very much effective for the applications, specially, where the reduction of subthreshold leakage power dissipation in standby mode is warranted for.

VI. CONCLUSION

Subthreshold leakage power reduction in standby mode is very much essential for burst mode type circuits, where computation occurs only during short burst intervals, and the system is in standby mode for the majority of the time. The wastage of useful battery power during long standby period is highly undesirable. Portable elec- tronic appliances such as cell phones and pagers are used in active mode for a very short time interval. These ap- pliances drain their useful battery power for a very long standby period. Similarly, the leakage of battery power in portable laptop during standby mode is highly undesirable. Subthreshold leakage reduction techniques during the standby mode can significantly reduce the leakage in burst mode applications. The proposed hybrid stack technique proved to perform better in terms of lower subthreshold leakage power dissipation in standby mode in comparison with other existing techniques.

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