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Comparative Analysis of Fast Motion Estimation Algorithm for Design of VLSI Processors

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ABSTRACT: This paper presents a flexible and scalable motion estimation processor capable of supporting the processing requirements ,which is suited for FPGA implementation. Our core is optimized to execute all existing fast block matching algorithms, which we show to match or exceed the inter-frame prediction performance of traditional full-search approaches at the HD resolutions commonly in use today. We propose to implement a motion estimation algorithm in FPGA Processor. The proposed system will be designed using Verilog HDL and simulated using Modelsim Software.

KEYWORDS: Motion estimation, comparative analysis, VLSI design, video processing, hardware acceleration, algorithm optimization, digital signal processing, computational efficiency, FPGA implementation, image compression

I. INTRODUCTION

Video coders compress digital video sequences by removing redundancies. The most important redundancy temporal redundancy—is typically reduced by motion estimation and motion compensation which encodes the differences between intensity values in the current frame and those of their counterparts in the reference frame that has been translated by an estimated motion vector. In most video coding standards, motion estimation is block based. A video frame is divided into nonoverlapping macroblocks, typically of size 16* 16 pixels. Each macroblock is compared to candidate blocks within a search area in the reference frame.

This process is referred to as the block matching algorithm (BMA). Various distortion measures could be used for finding the best match for a macroblock in the motion estimation process. Mean squared error (MSE), mean absolute error (MAE), and sum of absolute differences (SAD) are commonly used.

II. RELATED WORK

Recently, a new distortion measure for motion estimation has been proposed—the sum of absolute transformed differences (SATD) [1]. This measure sums the frequency transform coefficients, typically the Hadamard transform, of the differences between the pixels in the template macroblock and the corresponding pixels in a candidate block. SATD is considerably slower than the SAD but it more accurately predicts quality from the viewpoints of both objective and subjective metrics. Therefore, it is used in the H.264 reference model software [2], as well as in other new video encoders. Motion estimation, although efficient in reducing temporal redundancy, incurs high computational complexity. A full search technique for finding the best matching region within the search area in the reference frame is usually impractical for real-time applications due to the large number of comparisons required. Thus, many alternative “fast search” motion estimation algorithms have been proposed in the literature. The main concepts of these fast algorithms can be classified into six categories: reduction in search positions, predictive search, simplification of matching criterion, bitwidth reduction, hierarchical search, and fast full search [3]. The most popular category is the reduction in search positions. Algorithms in this category reduce search complexity by limiting the number of candidate blocks. These algorithms rely on the assumption that the matching error monotonically increases with the distance from the optimal position (having minimum distortion). This assumption is not always valid and the process may converge to a local minimum on the error surface rather than to the global minimum as in the full search algorithm. Well-known algorithms in this category are the 2-D logarithmic search, three-step search, four-step search, cross search, diamond search, and center-biased diamond search. Diamond search based algorithms have significantly better performance in speed and quality than prior algorithms. However, due to its simplicity, three-step search is still commonly used.

Predictive motion estimation, for example [10] and [11], utilizes the motion information in the spatial and/or temporal neighboring macroblocks to form an initial estimate of the current motion vector; thus, it can effectively reduce the search area as well as the computation. Another approach for fast motion estimation is to speed up the calculation of matching error for each candidate block independently. This is usually achieved by subsampling the pixels in the template and candidate blocks [12], [13]. Finding the optimal match withminimum matching error using this technique is, however, not guaranteed. This approach may be combined with the former two techniques to limit the number of search positions and to predict the current motion vector. A different approach for fast motion estimation uses simple matching criteria to reject search positions while ensuring theglobal minimal matching error can still be attained. Only candidate blocks that have not been disqualified are further processed using more precise distortion calculations. Using an appropriate test, many search positions may be excluded from being further considered in the motion vector search, thus reducing search complexity significantly.

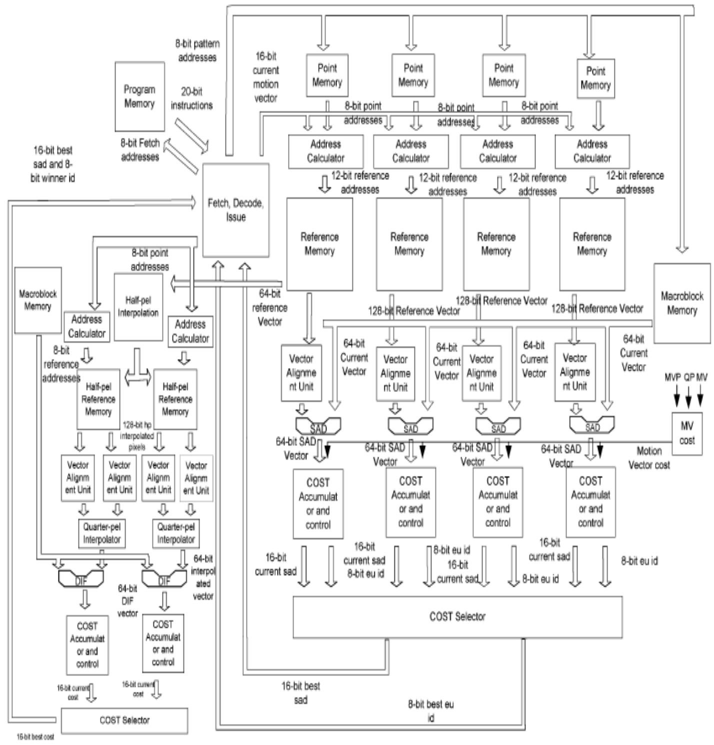
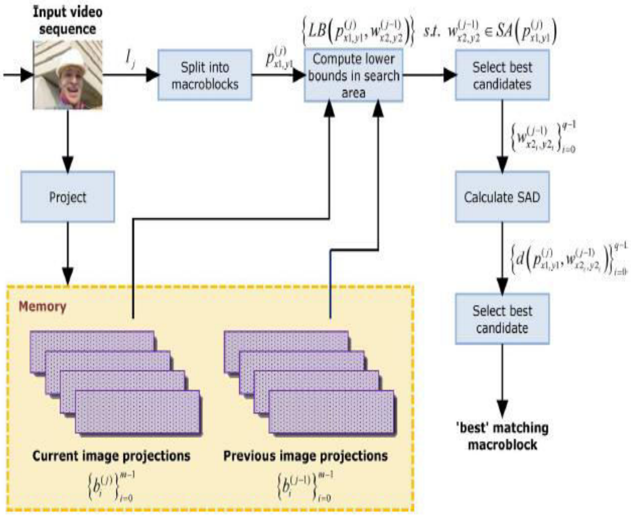
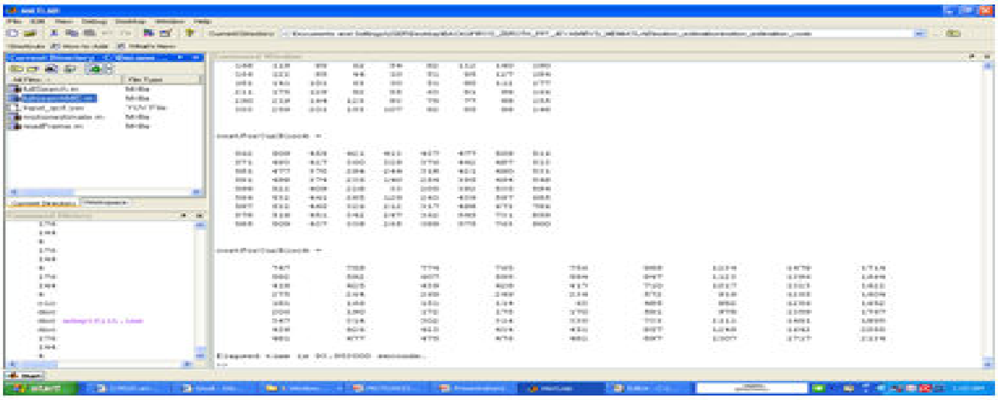


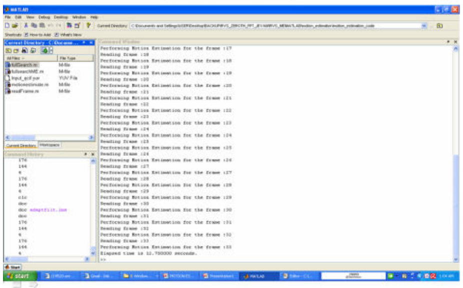
Fig. 6. Microarchitecture with a total of seven execution units.



ESTIMATING ME TIME FOR 33 FRAMES VIDEO WITH DISPLAYING THE COST



ESTIMATING ME TIME FOR 33 FRAMES VIDEO WITH OUT DISPLAYING THE COST
(block window size:4)



```
Performing Motion Estimation for the frame :17
Reading frame :18
Performing Motion Estimation for the frame :18
Reading frame :19
Performing Motion Estimation for the frame :19
Reading frame :20
Performing Motion Estimation for the frame :20
Reading frame :21
Performing Motion Estimation for the frame :21
Reading frame :22
Performing Motion Estimation for the frame :22
Reading frame :23
Performing Motion Estimation for the frame :23
Reading frame :24
Performing Motion Estimation for the frame :24
Reading frame :25
Performing Motion Estimation for the frame :25
Reading frame :26
Performing Motion Estimation for the frame :26
Reading frame :27
Performing Motion Estimation for the frame :27
Reading frame :28
Performing Motion Estimation for the frame :28
Reading frame :29
Performing Motion Estimation for the frame :29
Reading frame :30
Performing Motion Estimation for the frame :30
Reading frame :31
Performing Motion Estimation for the frame :31
Reading frame :32
Performing Motion Estimation for the frame :32
Reading frame :33
Performing Motion Estimation for the frame :33
Elapsed time is 12.750000 seconds.
>>
```

FOR 33 FRAMES VIDEO

NAME OF THE VIDEO	BLOCK WINDOW SIZE	ME TIME IN SEC
Input_qcif	4	12.75
Input_qcif	5	17
Input_qcif	8	60

III. SIMULATION RESULTS

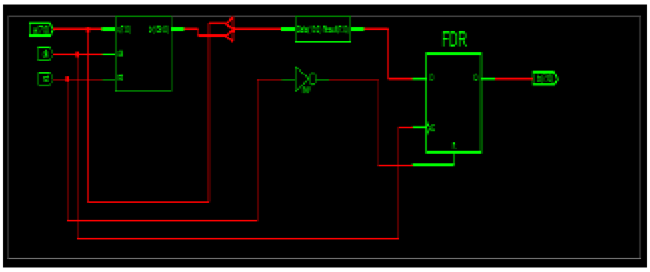


Fig.RTL View of Proposed Architecture

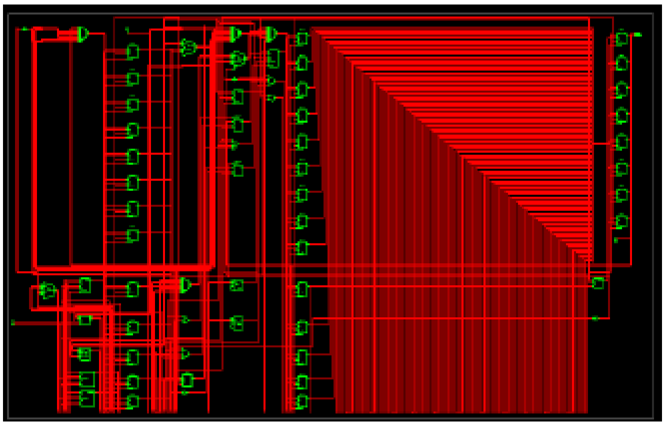
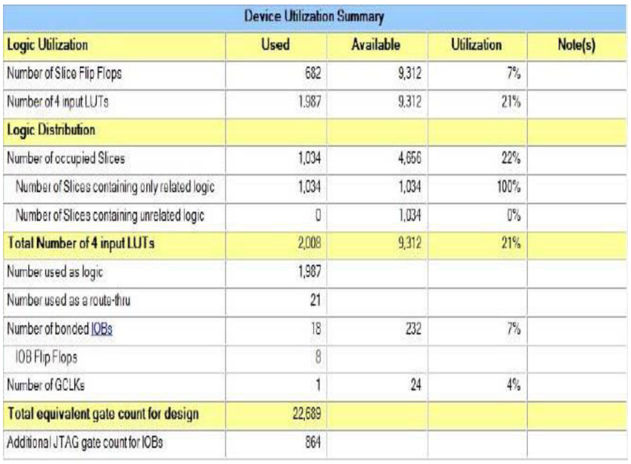


Fig. Technology Schematic View



Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	682	9,312	7%	
Number of 4 input LUTs	1,987	9,312	21%	
Logic Distribution				
Number of occupied Slices	1,034	4,656	22%	
Number of Slices containing only related logic	1,034	1,034	100%	
Number of Slices containing unrelated logic	0	1,034	0%	
Total Number of 4 input LUTs	2,008	9,312	21%	
Number used as logic	1,987			
Number used as a route-thru	21			
Number of bonded IOBs	18	232	7%	
IOB Flip Flops	8			
Number of GCLKs	1	24	4%	
Total equivalent gate count for design	22,689			
Additional JTAG gate count for IOBs	864			

IV. CONCLUSION

The main features of the presented processor are the support of arbitrary fast motion estimation algorithms for real-time HD support, the seamless integration of fractional and integer-pel support, the availability of a software toolset to ease the development of new motion estimation algorithms and processors and the description of a scalable, configurable architecture with a variable number of execution units determined by algorithmand throughput requirements. The combination of these features constitutes a significant advancement compared with the work reviewed in Section II. When compared to traditional full hardware, the presented core scales well to large search ranges without linear increases in hardware resources and consequently power consumption. When compared to other ASIPprocessors, our work is faster, more scalable, and fully supports the advanced features introduced with the H.264 standard. The measured power values have been added to the cycle accurate simulator part of the toolset1 which can then be used to configure the processor according to power, performance, and complexity constraints.

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