



Design of Sequential Elements for Low Power Clocking System

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ABSTRACT: A large portion of the on chip power is consumed by the clock system which is made of the clock distribution network and flip-flops. So the objective is to reduce the power consumption. A method of “Conditional Data Mapping Flip Flop” (CDMFF) was proposed earlier. The drawbacks of CDMFF are it uses more number of transistors and it has a floating node on its critical path. Moreover it cannot be used in noise intensive environment. So we propose a method called “Clocked Pair Shared Implicit Pulsed Flip Flop” (CPSFF) here. In this method the number of transistors are reduced by sharing the clocked pair transistors. The design is implemented in MICROWIND 3.1. Analysis of the performance parameters shows that performance of CPSFF is superior compared to conventional flip flop. The overall power is reduced in CPSFF when compared to the previous method CDMFF.

KEYWORDS: CDMFF , CPSFF.

I. INTRODUCTION

The System-On-Chip (SoC) design is integrating hundreds of millions of transistors on one chip, whereas packaging and cooling only have a limited ability to remove the excess heat. All of these results in power consumption being the bottleneck in achieving high performance and it is listed as one of the top three challenges in ITRS 2008. The clock system, which consists of the clock distribution network and sequential elements (flip-flops and latches), is one of the most power consuming components in a VLSI system. It accounts for 20% to 40% of the total power dissipation in a system.

As a result, reducing the power consumed by flip-flops will have a deep impact on the total power consumed. A large portion of the on chip power is consumed by the clock drivers. Caution must be paid to reduce clock load when designing a clocking system. There is a wide selection of flip-flops in the literature. Many contemporary microprocessors selectively use master-slave and pulsed-triggered flip-flops. Traditional master-slave single-edge flip-flops, for example, transmission gated flip-flop, are made up of two stages, one master and one slave. Another edge-triggered flip-flop is the sense amplifier-based flip-flop (SAFF).

All of these hard edged-flip-flops are characterized by a positive setup time, causing large D-to-Q delays. Alternatively, pulse-triggered flip-flops reduce the two stages into one stage and are characterized by the soft edge property. 95% of all static timing latching on the Itanium 2 processor use pulsed clocking.

Pulse triggered flip-flops could be classified into two types, implicit-pulsed and explicit-pulsed, for example, the implicit pulse-triggered data-close-to-output flip-flops (ip-DCO) and the explicit pulse-triggered data-close-to-output flip-flops (ep-DCO).

A transmission-gate master-slave latch pair has the largest internal race margin, lowest energy consumption, and has energy-delay product comparable to much faster pulse-triggered latches. A common design approach for minimizing energy consumption in flip-flops is to reduce the switching component of energy,

$$E = a.C_{sw}.V_{swing}.V_{DD}.$$



Based on this formula, energy consumption can be reduced by simply minimizing each of the terms in the product expression. However, lowering the supply voltage results in increased flip-flop delay, so the delay has to be included in the optimization metric. Clocked capacitances should be minimized in order to reduce the clock load. The total circuit area depends on the size of the output load and required driving strength. With energy reduction in clocked nodes and the output load, sizing for optimal performance under these energy constraints reduces to optimizing the speed of the flip-flop's critical path. This closely approximates the sizing for optimal energy-delay product (EDP). The circuit is optimized to drive an output load of 4 standard loads (SL), where SL is the input capacitance of a unity buffer from standard cell library. While 4SL load is most common effective fan-out in synthesized low energy systems, sizing procedure can be extended to any load. The method of logical effort is used in transistor size optimization.

The rest of the paper is organized as follows. Section II describes the implementation of our identification method. Section III presents experimental results that illustrate the effectiveness of this approach. Section IV compares the results with existing method and the Section V includes the concluding remarks.

II. CONDITIONAL DATA MAPPING FLIP-FLOP

A. Methods of Low Power Design of a Clocking System

In Power consumption is determined by several factors including frequency f , supply voltage V , data activity α , capacitance C , leakage and short circuit current

$$P = P_{\text{dynamic}} + P_{\text{short circuit}} + P_{\text{leakage}}$$

In the above equation, dynamic power P_{dynamic} is also called the switching power,

$$P_{\text{dynamic}} = \alpha CV^2f.$$

P_{leakage} is the short circuit power which is caused by the finite rise and fall time of input signals, resulting in both the pull up network and pull down network to be ON for a short while. $P_{\text{short circuit}} = I_{\text{short circuit}} V_{\text{dd}}$
 P_{leakage} is the leakage power. With supply voltage scaling down, the threshold voltage also decreases to maintain performance. However, this leads to the exponential growth of the subthreshold leakage current. Subthreshold leakage is the dominant leakage now.

$$P_{\text{leakage}} = I_{\text{leakage}} V_{\text{dd}}.$$

B. Factors that Lowering the power Consumption

Based on these factors, there are various ways to lower the power consumption shown as follows.

1) Double Edge Triggering:

Using half frequency on the clock distribution network will save approximately half of the power consumption on the clock distribution network. However the flip-flop must be able to be double clock edge triggered.

For example, the clock branch shared implicit pulsed flip-flop (CBS-ip DEFF), is a double edge triggered flip-flop. Double clock edge triggering method reduces the power by decreasing frequency f in equation.

2) Using a low swing voltage on the clock distribution network can reduce the clocking power consumption since power is a quadratic function of voltage. To use low swing clock distribution, the flip-flop should be a low swing flip-flop.

For example, low swing double-edge flip-flop (LSDFF) is a low swing flip-flop. In addition, the level converter flip-flop is a natural candidate to be used in low swing environment too. For example, CD-LCFF-ip could be used as a low swing flip-flop since incoming signals only drive nMOS transistors. The low swing method reduces the power consumption by decreasing voltage in equation.

3) There are two ways to reduce the switching activity: conditional operation (eliminate redundant data switching: conditional discharge flip-flop (CDFF)), conditional capture flip-flop (CCFF) or clock gating.

a) Conditional Operation:

For dynamic flip-flops, like hybrid latch flip-flop (HLFF), semidynamic flip-flop (SDFF), there are redundant switching activities in the internal node. When input stays at logic one, the internal node is kept charging and discharging without performing any useful computation. The conditional operation technique is needed to control the redundant switching.

For example, in CDFF, a feedback transistor is inserted on the discharging path of 1st stage which will turn off the discharging path when D keeps 1. Internal node will not be kept discharging at every clock cycle.

In CCFF, it uses a clocked NOR gate to control an nMOS transistor in discharging path when Q keeps 1. The redundant

switching activity is removed in both cases. This reduces the power consumption by decreasing data activity.

b) Clock Gating:

When a certain block is idle, we can disable the clock signal to that block to save power. Gated master slave flip-flop is used. Both conditional operation and clock gating methods reduce power by decreasing switching activity.

4) Using Dual Vt/MTCMOS to reduce the leakage power in standby mode. With shrinking feature size, the leakage current increases rapidly, the MTMOS technique as well as transistor stacking, dynamic body biasing, and supply voltage ramping could be used to reduce leakage standby power consumption .5) Reducing Short Current Power: Split path can reduce the short current power, since pMOS and nMOS are driven by separate signals.

6) Reducing Capacity of Clock Load:

80% of non clocked nodes have switching activity less than 0.1. This means reducing power of clocked nodes is important since clocked node has 100% activity. One effective way of low power design for clocking system is to reduce clock capacity load by minimizing number of clocked transistor. Any local clock load reduction will also decrease the global power consumption. This method reduces power by decreasing clock capacity.

C .Conditional Data Mapping Flip Flop

The Clock drivers consume large part of the on-chip power. It is desirable to have less clocked load in the system. Conditional Discharge Flip flop (CDFF) and Conditional Capture Flip flop (CCFF) both have many clocked transistors. For example, CCFF used 14 clocked transistors, and CDFF used 15 clocked transistors. In contrast, conditional data mapping flip-flop used only seven clocked transistors, resulting in about 50% reduction in the number of clocked transistors, hence CDMFF used less power than CCFF and CDFF. This shows the effectiveness of reducing clocked transistor numbers to achieve low power. CDMFF consumes less power than CCFF and CDFF. However, there is redundant clocking capacitance in CDMFF. When data remains 0 or 1, the pre-charging transistors, P1 and P2, keep switching without useful computation, resulting in redundant clocking. Clearly, it is necessary to reduce redundant power consumption here. Further, CDMFF has a floating node on critical path because its first stage is dynamic.

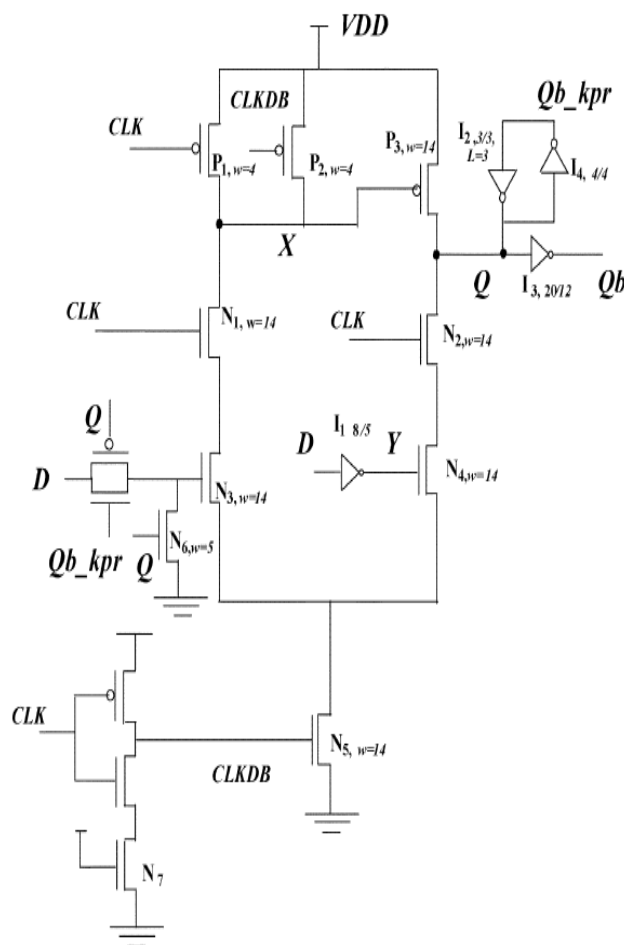


Fig.1. Conditional Data Mapping Flip Flop (CDMFF)



Comparing with CDMFF, a total of three clocked transistors are reduced, such that the clock load seen by the clock driver is decreased, resulting in an efficient design. Further the transistor N7 in the clocked inverter in CDMFF is removed. CPSFF uses four clocked transistors rather than seven clocked transistors in CDMFF, resulting in approximately 40% reduction in number of clocked transistors.

Furthermore the internal node X is connected to Vdd by an always on P1, so X is not floating, resulting in enhancement of noise robustness of node X. This solves the floating point problem in CDMFF. The always ON P1 is a weak pMOS transistor (length=31). This scheme combines pseudo nMOS with a conditional mapping technique where a feedback signal, comp, controls nMOS N1.

When input D stays 1, Q = 1, N 5 is on, N1 will shut off to avoid the redundant switching activity at node X as well as any short circuit current. pMOS P2 should pull Q up when D transits to 1. The second nMOS branch (N2) is responsible for pulling down the output of Q if D = 0 and Y = 1. When the clock pulse arrives, pMOS in I1 should turn on nMOS N2 when D = 0.

Although P1 is always ON, short circuit only occurs one time when D makes a transition of 0 to 1, and the discharge path is disconnected after two gates delay by comp (turning off N1). After that, if D remains at 1, the discharge path is already disconnected by N1; there would be no short circuit.

The clocked-pseudo-nMOS scheme is different from the general idea of conventional pseudo-nMOS logic in that we use clocked transistors in the pull down branch. P1, N1, N3, and N4 should be properly sized to ensure a correct noise margin.

Several low power techniques can be easily incorporated into the new flip-flop. Unlike CDMFF, low swing is possible for CPSFF since incoming low voltage clock does not drive pMOS transistors. Low swing voltage clock signals could be connected to the nMOS transistors N3 and N4, respectively. In addition, it is easy to build double edge triggering flip-flop based on the simple clocking structure in CPSFF. Further CPSFF could be used as a level converter flip-flop automatically, because incoming clock and data signals only drive nMOS transistors.

IV. RESULTS AND DISCUSSION

The simulation results of the circuits of the CDMFF and CPSFF are discussed in this chapter. The circuit is drawn and simulated using MICROWIND 3.1 tool and the technology used here is 90nm. The schematic diagram and the output waveforms are shown.

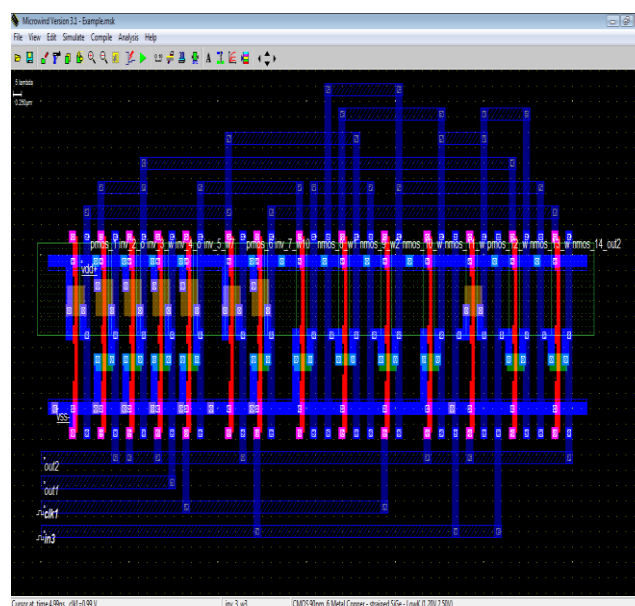


Fig. 3. Layout of CPSFF

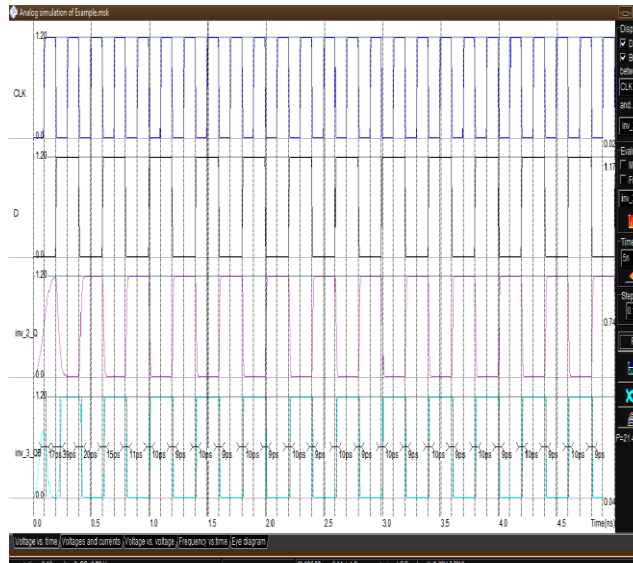


Fig.4. Waveform of CPSFF

The above figures shows the layout and the simulation output waveform of the CPSFF. The performance analysis and the comparison dissipation between the CDMFF and the CPSFF are shown in the table and figure.

Table 1 Performance comparison of CDMFF and CPSFF

PARAMETER	CDMFF	CPSFF
Power(μ W)	28.883	25.455
Delay(pS)	21.7	20.1
Power Delay Product (PDP) (E-15)	0.606	0.509

Fig. 3 shows the power dissipation of CPSFF. The power consumption of CPSFF decreases by 25%. The power consumption of proposed clock distribution system is also to be optimized. The performance parameter of the proposed design is measured and it is compared with conventional clocking system.

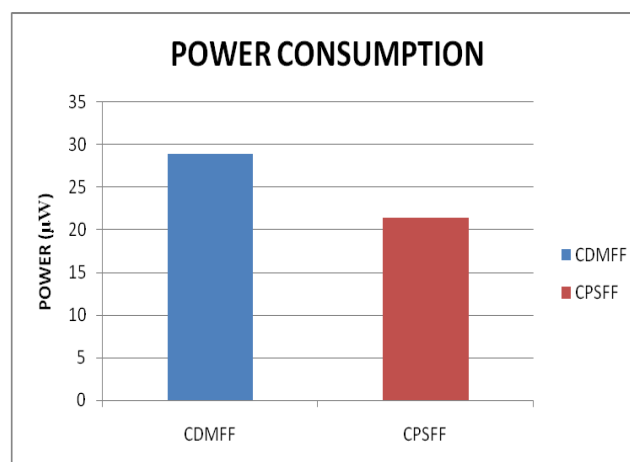


Fig.5. Power Analysis between CDMFF and CPSFF



V. CONCLUSION

The design of CDMFF and CPSFF is designed here. Using CDMFF, reducing capacity of the clock load by minimizing number of clocked transistor, is elaborated. Following the approach, the proposed CPSFF reduces local clock transistor number by about 40%. CDMFF and CPSFF are designed in MICROWIND 3.1. Comparison is made for CPSFF and CDMFF. outputs are verified for the input set and performance metrics for these methods are measured and tabulated. Analysis of result shows CPSFF outperforms CDMFF in terms of power dissipation and number of clocked transistors.

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