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# Carrier Overlapping PWM Method for Chopper Cell - Based Modular Multilevel Converters

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**ABSTRACT**: In this paper, carrier overlapping pulse width modulation (COPWM) method for chopper-cell (or half-bridge)-based modular multilevel converters (MMCs) is proposed. This method can generate an output voltage with maximally 2N+1 (where N is the number of sub modules in the upper or lower arm of MMC) levels, which is as great as that of the sub module unified pulse width modulation (SUPWM) method. However, no phase-shifted carrier is needed. Compared with the existing sub module unified pulse width modulated (SUPWM) method, the level number of the output voltage is almost doubled and the height of the step in the staircase voltage is reduced by 50%. Meanwhile, the equivalent switching frequency in the output voltage is twice that of the SUPWM method. All these features lead to much reduced harmonic content in the output voltage.

**KEYWORDS**: Modular Multilevel Converters (MMC), Carrier Overlapping Pulse Width Modulation (COPWM), Voltage balancing

## I. INTRODUCTION

Constructing power converters that are suitable for medium to high voltage range applications is a great challenge for power electronics. To achieve this goal, many multilevel converters have been proposed. Among the existing circuits, the cascaded, diode-clamped, and capacitor-clamped topologies are usually recognized as the three most common types [2]–[6]. With regard to the cascaded topologies, for example, the cascaded H-bridge converters are generally modular, but they cannot be operated as back-to-back converters without the help of transformers. The diode-/capacitor-clamped topologies can be employed as inverters, rectifiers, or back-to-back converters. However, they are essentially not modular and are quite complex as the number of the output voltage level increases.The modular multilevel converter (MMC), which is highly suitable for medium to high voltage applications, has attracted much research interest. The MMC can be used as a high-voltage inverter, rectifier, or four-quadrant converter, without bulky transformers. Actually, many academic papers have been published on MMC [5]–[20] in recent years. These papers mainly focus on modeling, pulse width modulation (PWM), voltage balancing, digital control, loss analysis, low-frequency operation, simulation techniques. In the proposed method, COPWM method has been used for multilevel inverter by using multiple carrier. Multi level inverter can produce many multilevel carrier based PWM method. Commonly there are 3 types of COPWM methods namely 1) Phase disposition (PD), 2) Phase opposition disposition (POD) and 3) Alternative phase opposition disposition method. [22] To improve the performance of the SUPWM method, this paper presents COPWM method with which the number of voltage levels can be as great as that with the SUPWM. Meanwhile, the height of the staircase output voltage can be reduced by 50% compared with the existing SUPWM method. Simulation results have both been presented to justify the presented method.

## II. SYSTEM DESCRIPTION

A.SUPWM METHOD FOR MMC

Fig. 1 shows one phase of MMC as an inverter where $U_{dc}$ is the dc-link voltage, $SM_{U\,1}$–$SM_{UN}$ and $SM_{L1}$–$SM_{LN}$ are the N sub modules in the upper and lower arms, respectively, $L_U$ and $L_L$ are the two buffer inductors in the upper and lower arms,

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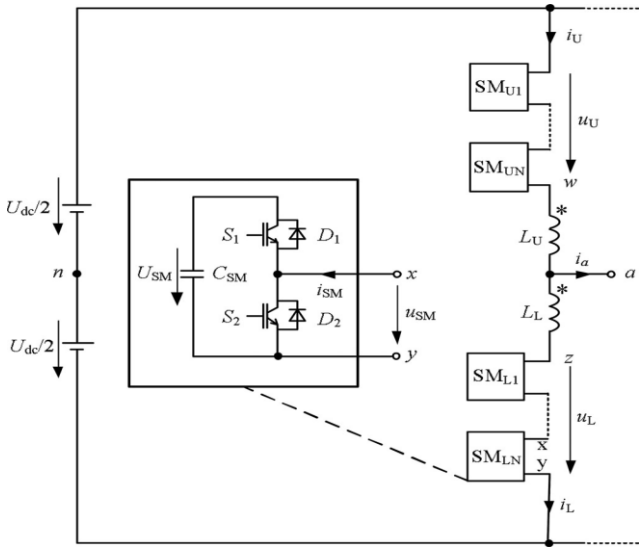


Fig 1. One arm of MMC- based inverter

$u_U$ and $i_U$ are the voltage and current of the upper arm, $u_L$ and $i_L$ are the voltage and current of the lower arm. The two buffer inductors can be selected as separate ones or coupled ones. The use of coupled inductors will result in considerable reductions in size, weight, and cost to the magnetic core [6], [11]. Therefore, this paper adopts coupled inductors. In Fig. 1, if $S_1$ is on and $S_2$ is off, the capacitor of this sub module will be connected in the arm irrespective of the direction of $i_{SM}$ and this state of the sub module is defined as IN. If $S_2$ is on and $S_1$ is off, the capacitor of this sub module will be bypassed and out of the arm irrespective of the direction of $i_{SM}$ and this state of the sub module is defined as OUT. With the SUPWM method, there will always be N sub module capacitors selected as IN.

## III. PROPOSED METHOD

A. COPWM Method

The COPWM method can balance the capacitor voltages of the sub modules with no dedicated close-loop controller and almost zero voltage stress on the buffer inductor. [9]. With the presented COPWM method, the number of output voltage level can be as great as that with the SUPWM method, but still no close-loop voltage balancing controller is needed. This is illustrated by Fig.3 in which the sub modules in the upper and lower arms all use the same carrier, i.e., $C_1$ and $C_2$ are of the same phase. Sub module selection algorithm and the reference voltages calculation for the switching sub modules in the upper and lower arms are the same as those of SUPWM method. However, this little change in the carrier phase will lead to substantially increased voltage level.

B. Mechanism of Increasing Output Voltage Level

With the COPWM method, as shown in Fig. 3, one can see that the number of IN state sub modules in the upper arm will be $K_1$ or $K_1$+ 1 while that in the lower arm will be N – $K_1$ –1or N – $K_1$.(where $k_1$ is a positive integer). However, the number of IN state sub modules will not be constantly N as with the SUPWM method, but will be N –1, N or N + 1.As the SUPWM method can output maximally N+1 levels, the COPWM method can introduce maximally N new levels. Therefore, the proposed method will have 2N+1 levels in the output voltage, which is almost double that of the SUPWM method. It is also clear from Fig. 3 that the height of the staircase in $u_{an}$ is $U_{SM}/2$, meaning 50% reduction compared with the SUPWM method as shown in Fig. 2. Meanwhile, $u_{an}$ switches twice within one Tc in Fig. 3, i.e., the equivalent switching frequency of $u_{an}$ is twice the carrier frequency, which means a 100% increase in the equivalent switching frequency compared with the SUPWM method. The reduced step height together with the increased equivalent switching frequency will lead to considerable suppression of voltage harmonics and dv/dt caused electromagnetic interference noise. It should be pointed out that the increased voltage levels can be obtained thanks to the coupled inductors. The coupled inductors in fact act as an adder/ subtracted of the upper and lower arm voltages. Thus, an extra voltage level can be produced. If the buffer inductors are separate, the 2N+1 levels cannot be obtained clearly for the influence of the circulating current between the dc link and the arms [6].

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c. Influences on Voltage Balancing of the Sub modules

The COPWM method actually not influences the selection of IN or OUT state sub modules as calculated by the SUPWM method. Only the phase of the carrier for the sub modules in the lower arm is changed. Therefore, the voltage balancing algorithm in the SUPWM method is still valid with the COPWM scheme and no close-loop voltage balancing controller is needed. Obviously, the voltage on the buffer inductors will be $-U_{SM}$,0 or $U_{SM}$ with the COPWM method

TABLE I Parameters Of The MMC-Based Single Phase Inv Enter For Simulation

| | |
|---|---|
| DC-link voltage | $U_{dc}$=3000 V |
| Submodule capacitor voltage ref. | $U_{SM\_ref}$=600 V |
| No. of submodules in upper/lower arm | $N$=5 |
| Submodule capacitor | $C_{SM}$=3 mF |
| Buffer inductors | $L_U$= $L_L$=$M$=2 mH |
| Carrier frequency | $f_{carrier}$=2 kHz |
| Output voltage ref. | $u_{an\_ref}$=1440cos(100$\pi t$) V |
| Load resistance | $R_{Load}$=100 Ω |
| Load inductance | $L_{Load}$ =10 mH |

while that with the SUPWM method is zero ideally. The voltage stress on the buffer inductors seems larger with the proposed approach. However, the power switches are not ideal and dead time must be added to the gating signals in reality. If the dead time effect is considered, high-voltage narrow-pulses will be imposed on the buffer inductors. With the COPWM method, the level number of the output voltage can be as great as that with the SUPWM method. The differences between the two methods are also apparent. First, the SUPWM method modulates each sub module separately with 2N phase-shifted carriers while with the COPWM method the carriers for the sub modules are all the same. The 2N+1 voltage levels are obtained by the phase-shifted carriers in the SUPWM, but the COPWM method achieves this goal via the coupled inductors. Second, with the CPSPWM method, dedicated capacitor voltage balancing controllers for each sub-module are mandatory [11], [18] while the COPWM method does not need any close-loop controller for balancing sub module capacitor voltages.

## IV. SIMULATION RESULTS

In order to verify the validity of the proposed method in this paper, an MMC-based single-phase inverter is taken as the test example. The setup of the inverter for simulation and experiment is shown in Fig. 1. Computer simulation is carried out first in MATLAB/Simulink software and the parameters are listed in Table I. Figs 3 & 4 show the simulation results. It is seen from Fig. 3 that the output voltage level increases from 6 to 11 after 0.06 s and the height of the step in the output voltage reduces from 600 to 300 V. As a result, the ripple current in the load current has been substantially suppressed. The spectrum of $u_{an}$ with both methods is also displayed in Fig. 4 Obviously; the lowest harmonics is around the carrier frequency $f_{carrier}$ with the SUPWM method as shown in Fig. 4(a) while around the $2f_{carrier}$ with the COPWM method as shown in Fig. 4(b). These results match the theoretical analyses well. With the COPWM method as shown in Fig. 4(b), the harmonic of the highest amplitude at $f_{carrier}$ with the SUPWM method in Fig. 4(a) is eliminated although the harmonics around $f_{carrier}$ exist. This is because the voltages of the sub module capacitors are not constant as ac currents flow through them [8] and sub harmonics are introduced to $u_{an}$. The total harmonic distortion (THD) of $u_{an}$ decreases meaning substantial improvement in the output voltage quality.

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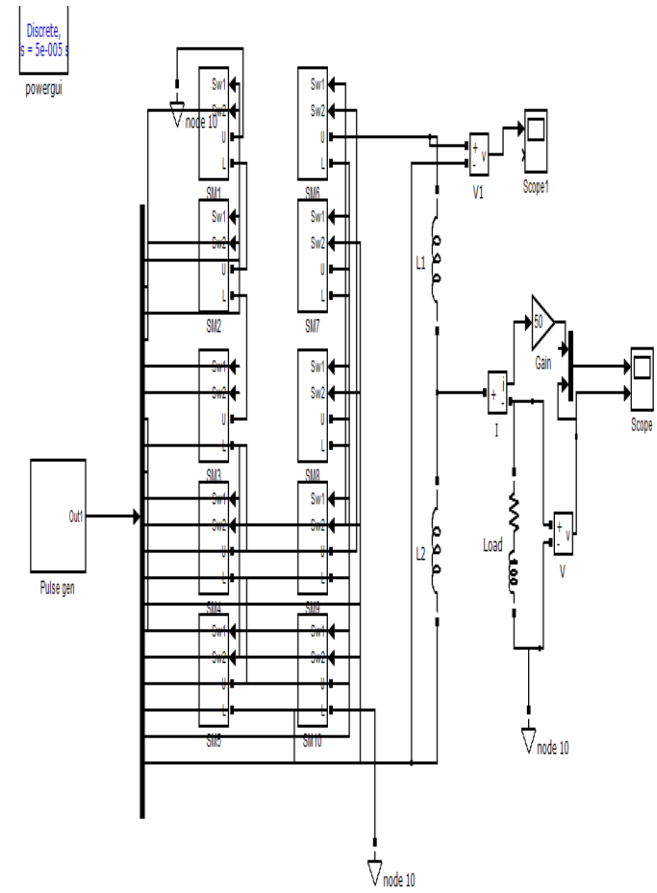


Fig.2: simulation diagram of the proposed model

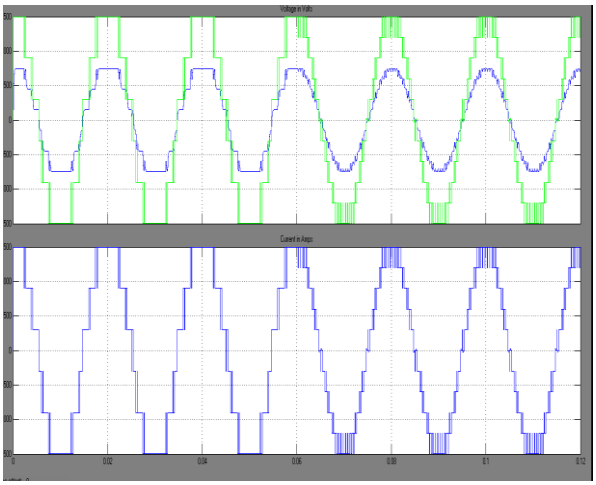

Fig.3. output voltage (green line) and load current x 50 (blue line ). The SUPWM method is adopted when t < 0.06 sec and COPWM method is adopted t ≥0.06 sec.

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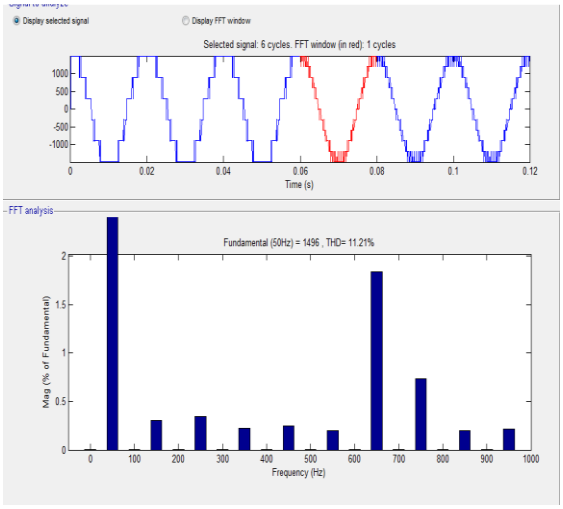


Fig.4.a THD of the output voltage with SUPWM method

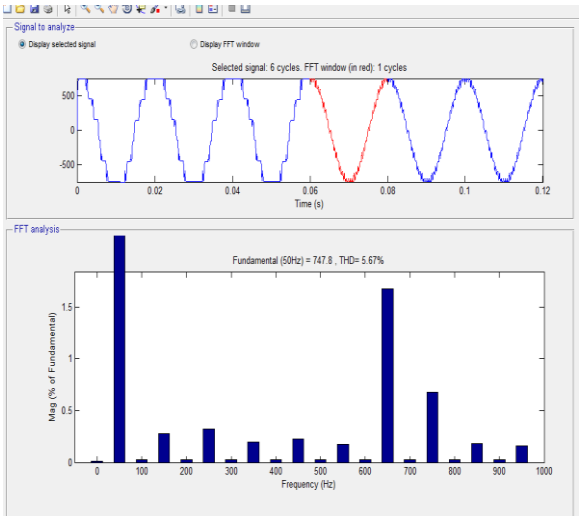


Fig4.b THD of the output voltage with COPWM method

## V. CONCLUSION

This paper proposed an COPWM method for chopper-cell based MMCs. The proposed method can output maximally 2N+1 voltage levels in the output voltage, which is almost double that with the SUPWM method. The equivalent switching frequency of the output voltage is doubled compared with SUPWM method. The sub module capacitor voltages can be well balanced with the COPWM method. The average voltage on the buffer inductors can also be kept at zero within each carrier period. Simulation results proved the validity of this method.

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