



# $2^{n+1}-1$ Level Multilevel Inverter using Reverse Voltage Technique with Reduced Number of Switches

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**ABSTRACT:** Multilevel Inverters are used for High Power, High Voltage applications. Multilevel Inverter has more number of switches, Voltage sources, complex PWM and voltage balancing problems. In this paper a novel topology of combination of Reverse voltage component and  $2^n$  voltage sources are effectively used to generate 31 level with reduced number of switches for higher voltage level and also the carrier signals and gate drives are reduced. Hence this topology is Economical for use with higher voltage levels.

**KEYWORDS:** Multilevel Inverter,  $2^n$  varying voltage sources, Power Electronics, MPWM, Topology.

## I. INTRODUCTION

Multilevel power conversion introduced two decades ago. Multilevel Inverters make use of higher number of switches in order to produce small voltage steps for higher voltage levels.  $dv/dt$  stress on the load has been reduced with smaller voltage steps and hence electromagnetic compatibility concerns [1].

Recent trend is the best utilization of the multilevel inverter with reduced number of switches and complexity in the control strategies. The mostly used multilevel inverters are cascade converter, neutral point clamped (NPC) inverter and flying capacitor inverter.

These converters are well aided in Industrial drives, FACTS (Flexible Ac Transmission System) and Vehicle propulsion [10], [11]. Multilevel inverters are suitable for renewable photovoltaic energy where the power quality and efficiency are much needed [12].

The voltage sources are not properly used in generating output voltage levels. The topology in [19] can generate only five output levels with four dc sources, while conventional Multilevel inverter can generate upto nine levels with the same number of power supplies.

In a new approach [13] make use of minimum dc sources and inserting transformer instead. Inclusion of transformer in the topology increases the overall cost and volume of the inverter.

A new topology has been introduced for Multilevel inverter with reduced number of components compared with the other types of MLI. This topology requires lesser number of switches to be operated in high switching frequency. Thus the control strategy is more reliable and simpler. A general method of multilevel modulation Phase disposition (PD) MPWM is applied to the inverter.

This paper presents a 31 level multilevel inverter with much reduced voltage sources and switches for higher voltage level. Thus when applied for higher voltage levels it is more reliability and much reduced cost.

## II. NOVEL MULTILEVEL INVERTER

### A. General description

Multilevel inverters are in general uses high frequency switches to be operated in both positive and negative polarities. There is no need to utilize all the switches for generating bipolar levels [1]. This topology is a combination of  $2^n$  voltage sources, level generation unit and polarity generation unit.

The adjacent switches are supplied in the ratio of  $2^n$  where  $n$  is the level generation unit. The level generation unit produces the required voltage levels in the unipolar mode. This unit requires high frequency switches for its operation. The Polarity generation unit is responsible for generating the required output voltage polarity. This unit makes use of low frequency switches which operates at reference frequency.

The positive voltage levels are generated by the high frequency functioned level generation unit and then it is fed to a Full bridge polarity generation unit where the required output polarity are produced. Thus this type of arrangement decreases the semiconductor switches needed to produce output voltage levels in positive and negative polarities.

The novel topology is 31 levels is shown in figure 1. This topology requires 4 high frequency main switches, 4 low frequency switches, 4 main diodes, 8 by passing diodes and 4 isolated dc sources for 1 phase system. The Multilevel inverter's left stage produces the required output levels without polarity and the right side stage produces the polarity for the output voltage.

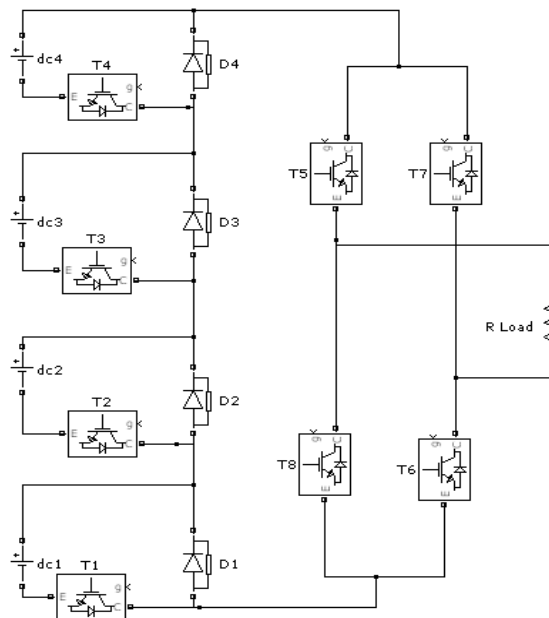


Fig. 1 Circuit diagram of the proposed MLI

The polarity generation unit reverses the voltage direction when voltage polarity to be changed for negative polarity. The function of the diodes is to avoid the short circuit of the DC sources. The DC sources are maintained in adjacent levels as 1: 2: 4: 8.

According to the required output voltage levels, the adjacent dc sources are linked or combined as per their requirements. When compared with the Reverse voltage (RV) topology [1] it requires only 4 Dc sources whereas the RV topology [1] requires 15 Dc sources for generating 31 levels in the output voltage. Thus it is superior to that of the RV topology.

Hence this topology requires fewer components compared with the conventional inverters and RV topology. The main advantage of this topology is that it requires only half of the conventional carriers for MPWM controllers. MPWM carriers for 31 level conventional inverters requires 30 carriers and for this novel topology it needs only 15 carrier as shown in figure 4. The Multilevel inverter with much reduced number of carriers is a great achievement for inverter control. Hence all the switches are not fast switches, the level generation unit only has fast switches and the polarity generation unit make use of slow switches.

B. Switching sequence

The switching sequences of this inverter are easier, since it does not generate negative pulses for negative cycle control. The switching sequence for each level is presented in the Table-I.



TABLE I Switching Sequences

Level	T1	T2	T3	T4
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

According to the table – I the required output voltage level is achieved by connecting the corresponding adjacent isolated voltage sources with the switches. The switching modes are chosen in such a way as to avoid unwanted voltage levels during switching cycles. It aids in reducing the switching power dissipation.

In accordance to the output voltage level 0 to 15 the sequence of switches are as shown in table – I. To produce 31 levels an embedded program has been coined in a microcontroller. In order to improve the efficiency of the inverter during switching states, the transition between modes in each state requires minimum commutation of switches.

The number of switches in proposed topology that conducts the circuit current is lower than that of cascade inverter and hence it has a much better efficiency. These switching sequences can be implemented by embedded program by Microcontroller MCT2E. The signals stage should be isolated from the power stage by optocouplers for control circuits. The driver is also responsible to generate the dead time between each successive cycle across the DC source.

H- Bridge polarity unit at the output stage performs in forward and reverse modes. In the forward mode switches 5 & 6 are conducted to have a positive output polarity. The switches 7 & 8 are switched on for generating negative output polarity. Thus the polarity generating unit decides the output polarity.

The major advantage of the topology is that it requires less high frequency switches. The high frequency switches and diodes are expensive and are more prone to be damaged than low frequency switches. According to the MIL-HDBK-217F standard the reliability of a system is indirectly proportional to the number of its components.

As the number of high frequency switches is increased the reliability of the inverter is decreased. This topology is used in PV array system, UPS, Backup Inverter, FACTS & HVDC. The cost & space availability and complexity in the control strategy are greatly reduced for higher voltage levels.

Switching losses, dv/dt stress on the load, EMI (ElectroMagnetic Interference) and THD (Total Harmonic Distortion) are reduced further when comparing cascade inverter for higher voltage levels.

### III. SIMULATION RESULTS

This section presents the simulation results of the 1 Phase 31 level inverter with the proposed topology as shown in figure 2. This topology is used to generate 31 voltage levels for a resistive load. The output peak voltage is 230V(VPP). The switching frequency is 4 KHz. The PD SPWM is used as the control strategy for driving the gates of the IGBT's of high frequency switches (Level generation unit).

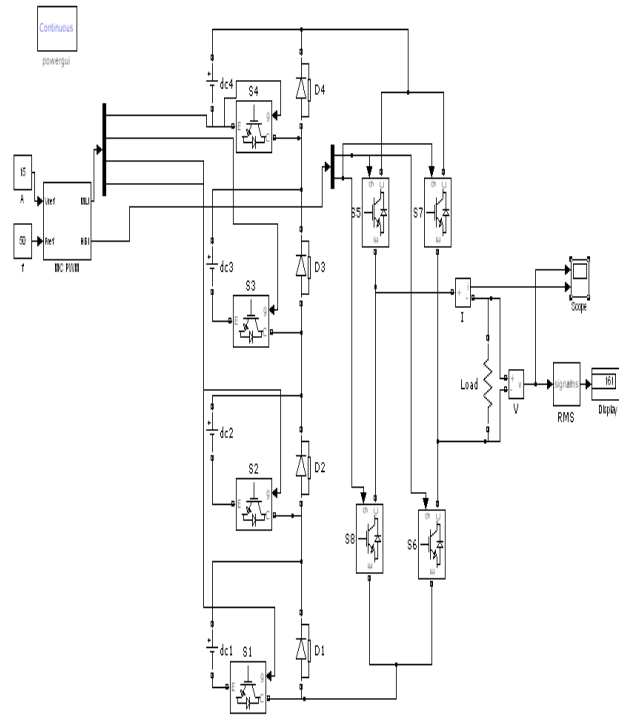


Fig. 2 New topology Multilevel inverter simulation diagram

Figure 3 shows the output voltage and output current. The proposed multilevel topology with an resistive load of  $100\Omega$  has a THD of 3.71% as shown in figure 5.

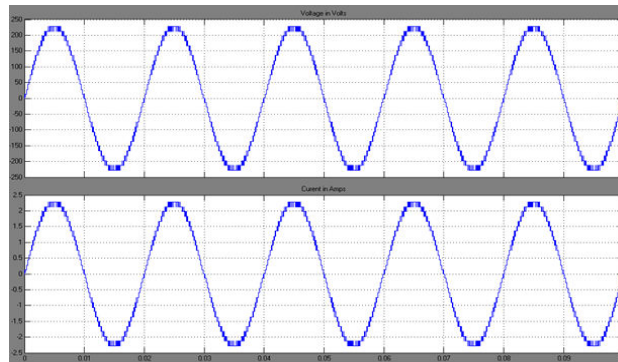


Fig .331 level output voltage & current waveforms of the proposed MLI.

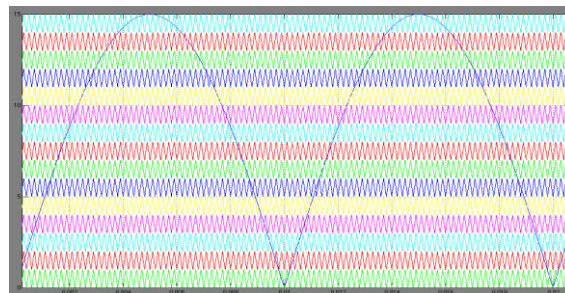


Fig 4 MCPWM carriers for Proposed topology

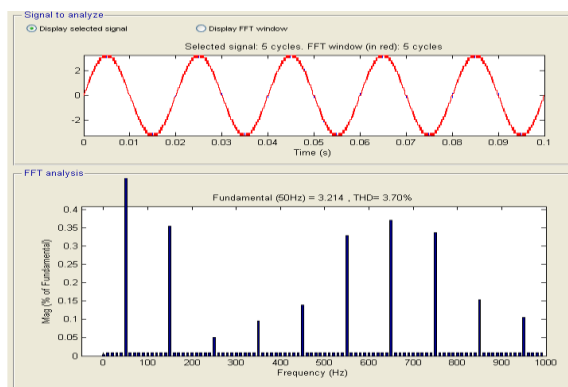


Fig5 FFT analysis of the proposed MLI

#### IV. CONCLUSION

In this paper a novel inverter topology has been proposed which is superior to that of cascade inverter in terms of power switches & isolated DC sources, control requirements, cost and reliability. Better selection for use in FACTS, HVDC, PV systems, UPS, etc; By separating the switching operations into high and low frequency parts, reduces the size and cost of the prototype.

The PD SPWM control method is used to drive the inverter. The PWM for this novel topology of multilevel inverter has much reduced number of carrier signals which facilitates in the reduction of complexities in the control strategy. Thus a novel topology of multilevel inverter with reduced number of switches, isolated dc source and few carriers for PWM has been proposed for further applications.

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