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Transformer -Less PV Inverter for Rooftop System

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ABSTRACT: This paper proposes the design of VLSI architecture for image fusion. To perform the process of image fusion VLSI architecture is designed using discrete wavelet transform (DWT) and it is implemented in Spartan 3EDK kit. The DWT architecture has the advantage of lower computational complexities and higher efficiencies. The algorithm is written in system C language and tested in SPARTAN-3 FPGA kit by interfacing a test circuit with the PC using the RS232 cable. In this proposed system, the coprocessor Microblaze is converted into a DWT architecture. The test results are seen to be satisfactory. It can overcome the shortages in previous works and high speed in processing for higher applications.

KEYWORDS: Discrete wavelet transform (DWT), image fusion,VLSI architecture

I. INTRODUCTION

Image fusion refers to the process of integrating information from different imaging modalities of a scene in a single composite image representation that is more informative and appropriate for visual perception or further processing [1].The images considered for fusion may be the images of the same object taken at different time or by different sensors. The aim of image fusion is to combine complementary and redundant information from multiple images to create a faster interpretation of the images. By using redundant information, image fusion may improve accuracy as well as reliability and by using complementary information, image fusion may improve interpretation capabilities with respect to subsequent tasks. According to above characteristics, image fusion leads more accurate data, increased utility and robust performance A large number of different image fusion methods have been proposed mainly due to the different available data types and various applications.A comprehensive survey of image fusion methods is available in [2], while a collection of papers was edited by Blum and Liu in [3]. For a dedicated review article on pixel-based image fusion in remote sensing refer[4],where related techniques of Earth observation satellite data are presented as a contribution to multisensory-integration-oriented data processing.

Image fusion in the spatial domain [5]–[7] have gained significant interest mainly due to their simplicity and linearity.Multiresolution analysis is another popular approach for image fusion [8]–[10], using filters with increasing spatial level in order to produce a pyramid sequence of images at different resolutions.In most of these techniques the high saliency pyramid values are taken from the transformed image and their inverse transform is found to get the fused image. In the fields of remote sensing, fusion of multiband images that lie in different spectral bands and corresponding areas of the electromagnetic spectrum is one of the key areas of research. The main target in these techniques is to produce an effective representation of the combined multispectral image data, i.e., an application-oriented visualization in a reduced data set [11]–[14].

II. RELATED WORKS

Jasiunas et al. [15] presented an image fusion system based on wavelet decomposition for unmanned airborne vehicles (UAVs). This is probably the first implementation developed on a reconfigurable platform alone, as well as the first investigation of adaptive image fusion that makes use of dynamic reconfiguration to change the fusion algorithm as the UAV approaches an object of interest.Results showed an achieved latency of 3.81 ms/frame for visible and infrared 8-bit images of 512 × 512 pixel resolution. Sims and Irvine presented in [16] an FPGA implementation using pyramidal decomposition and subsequent fusion of dual video streams.In [17], a real-time image processing system was presented for combining the video outputs of an uncooled infrared imaging system and a low-level-light TV system. Both images were 384 × 288 in size, with 8-bit resolution. The hardware implementation was based on a simple weighted pixel average and provided poor results regarding the contrast of the fused images. Aiming to provide enhanced results in both visual effect and image quality, Song et al. [18] proposed an alternative image fusion implementation based on Laplacian pyramid decomposition of two-channel VGA video fusion using parallel and pipelined architectures. In their work, a three-level Laplacian pyramid image fusion algorithm was implemented in VHDL according to the designed methods (including controlling, decomposing, fusion, and reconstruction modules). The design was verified on a real-time dual-channel image fusion system based on Virtex-4 SX35 FPGA, giving a fusion frame rate of 25 frames/s (real-time video). Li et al. [19] proposed an FPGA system of multisensor image fusion and enhancement for visibility improvement that can be used to help drivers driving at night or under bad weather conditions. Their design included wavelet-decomposition-based image fusion, as well as image registration and enhancement in order to improve the visibility of roads in extremely low lightning conditions.

III. SYSTEM ARCHITECTURE

In this proposed system the hardware implementation of the DWT is performed. For that,the coprocessor Microblaze is converted into DWT based image fusion architecture using Xilinx platform studio in system C language and then tested in Spartan 3EDK FPGA kit. The basic architecture used for this process as shown in figure

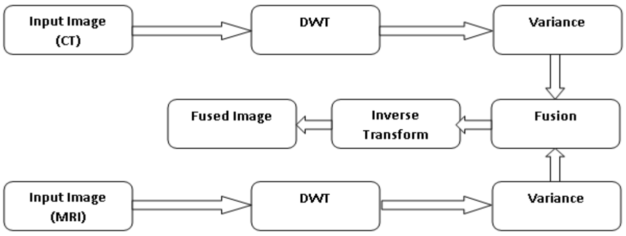


Fig 1.Basic architecture

First, the DWT of images is taken.After that, the fusion process is carried out using appropriate fusion rule .Finally, the inverse DWT gives the final fused image.

A. Microblaze processor design

The MicroBlaze embedded soft core is a reduced instruction set computer (RISC) optimized for implementation in Xilinx field programmable gate arrays (FPGAs). See figure 2 for a block diagram depicting the MicroBlaze core.FIELD PROGRAMMABLE GATE ARRAYS (FPGA's) are flexible and reusable high-density circuits that can be easily re-configured by the designer, enabling the VLSI design / validation /simulation cycle to be performed more quickly and less expensive. Increasing device densities have prompted FPGA manufacturers, such as Xilinx and Altera, to incorporate larger embedded components, including multipliers, DSP blocks and even embedded processors. One of the recent architectural enhancements in the Xilinx Spartan, Virtex family architectures is the introduction of the MicroBlaze (Soft IP) and PowerPC405 hard-core embedded processor.The MicroBlaze processor is a 32-bit Harvard Reduced Instruction Set Computer (RISC)

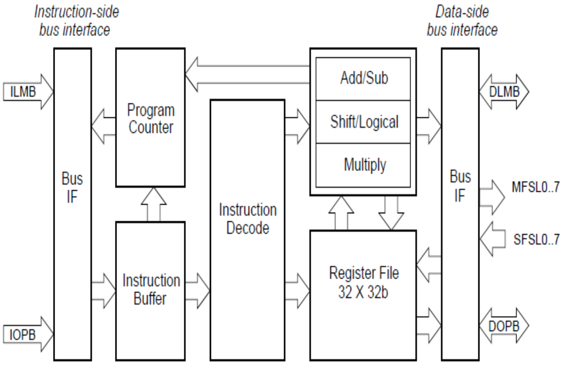


Figure 1-1: **MicroBlaze Core Block Diagram**

Fig 2. Micro blaze Core Block Diagram

architecture optimized for implementation in Xilinx FPGAs with separate 32-bit instruction and data buses running at full speed to execute programs and access data from both on-chip and external memory at the same time.

An interrupt controller is available for use with the Xilinx Embedded Development Kit (EDK) software tools. The processor will only react to interrupts if the Interrupt Enable (IE) bit in the Machine Status Register (MSR) is set to 1. On an interrupt the instruction in the execution stage will complete, while the instruction in the decode stage is replaced by a branch to the interrupt vector (address Ox 10). The interrupt return address (the PC associated with the instruction in the decode stage at the time of the interrupt) is automatically loaded into general-purpose register. In addition, the processor also disables future interrupts by clearing the IE bit in the MSR. The IE bit is automatically set again when executing the RTlD instruction.

Due to the advancement in the fabrication technology and the increase in the density of logic blocks on FPGA, the use of FPGA is not limited to anymore to debugging and prototyping digital circuits. Due to enormous parallelism achievable on FPGA and the increasing density of logic blocks, it is being used now as a replacement to ASIC solutions in a few applications. Soft cores are technology independent and require only simulation and timing verification after synthesized to a target technology.

B. Xilinx platform studio

The Xilinx Platform Studio (XPS) is the development environment or GUI used for designing the hardware portion of your embedded processor system. B. Embedded Development Kit Xilinx Embedded Development Kit (EDK) is an integrated software tool suite for developing embedded systems with Xilinx MicroBlaze and PowerPC CPUs. EDK includes a variety of tools and applications to assist the designer to develop an embedded system right from the hardware creation to final implementation of the system on an FPGA. System design consists of the creation of the hardware and software components of the embedded processor system and the creation of a verification component is optional. A typical embedded system design project involves: hardware platform creation, hardware platform verification (simulation), software platform creation, software application creation, and software verification. Base System Builder is the wizard that is used to automatically generate a hardware platform according to the user specifications that is defined by the MHS (Microprocessor Hardware Specification) file. The MHS file defines the system architecture, peripherals and embedded processors]. The Platform Generation tool creates the hardware platform using the MHS file as input.

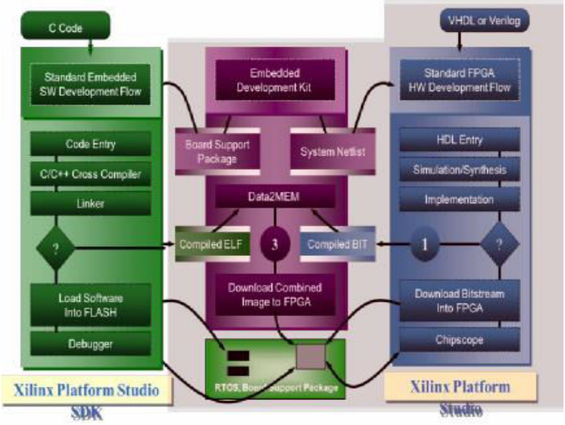


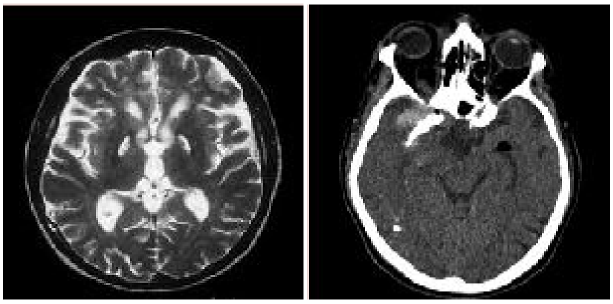
Fig 3. Embedded Development Kit Design Flow

The creation of the verification platform is optional and is based on the hardware platform. The MHS file is taken as an input by the Simgen tool to create simulation files for a specific simulator. Three types of simulation models can be generated by the Simgen tool: behavioral, structural and timing models. Some other useful tools available in EDK are Platform Studio which provides the GUI for creating the MHS and MSS files. Create / Import IP Wizard which allows the creation of the designer's own peripheral and import them into EDK projects. Bitstream Initializer tool initializes the instruction memory of processors on the FPGA. GNU Compiler tools are used for compiling and linking application executables for each processor in the system. There are two options available for debugging the application created using EDK namely: Xilinx Microprocessor Debug (XMD) for debugging the application software using a Microprocessor Debug Module (MDM) in the embedded processor system, and Software Debugger that invokes the software debugger corresponding to the compiler being used for the processor. C. Software

Development Kit Xilinx Platform Studio Software Development Kit (SDK) is an integrated development environment, complimentary to XPS, that is used for C/C++ embedded software application creation and verification.The software application can be written in a "C or C++" then the complete embedded processor system for user application will be completed, else debug & download the bit file into FPGA. Then FPGA behaves like processor implemented on it in a Xilinx Field Programmable Gate Array (FPGA) device.

IV. SIMULATION RESULTS

Experiments are performed on gray level images to verify the proposed method. These images are represented by 8 bits/pixel and size is 128 x 128. Image used for experiments are shown in below figure. The architectures were implemented in system C and placed and routed on Xilinx spartan3 XC3S200 FPGA, using Xilinx platform studio v.10.1



a b.

Fig 4. Input images a)MRI image b)CT image

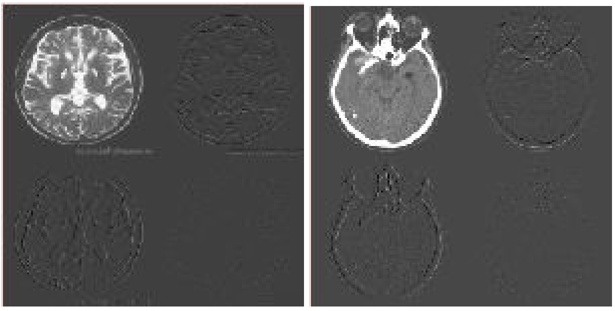


Fig 5. a)DWT of MRI image b) DWT of CT image

Fig 6. Output fused image

V. CONCLUSION

In this paper, an architecture for 2-dimensional DWT with its VLSI implementation has been proposed. Image fusion has attracted more attention due to increasing demands of clinical and other applications for they can support more accurate information than any individual source image. The architectures are representative of many design styles and range from highly parallel architectures. Here an average technique based reconfigurable system is designed using the EDK tool. Hardware architectures has been implemented as a coprocessor in an embedded system. In addition, the hardware cost of this architecture is compared for benchmark images. This type of work using EDK can be extended to other applications of embedded system.

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